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FM25LG01BI3

1.8V 1G-BIT SPI NAND FLASH MEMORY

Datasheet

Sep. 2024

Trademarks

1. Description

The FM25LG01BI3 is a 1G-bit (128M-byte) SPI (Serial Peripheral Interface) NAND Flash memory, with advanced write protection mechanisms. The FM25LG01BI3 supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O option.

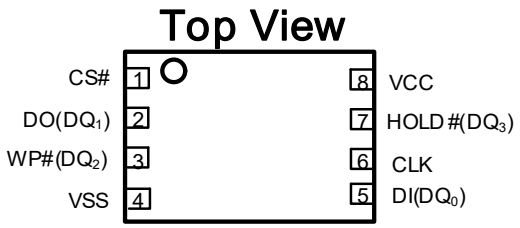
2. Features

- **1G-bit NAND Flash Memory**
  - Single-level cell (SLC) technology
  - Page size : 2176 bytes (2048 + 128 bytes)
  - Block size : 64 pages (128K + 8K bytes)
  - Device size : 1Gb (1024 blocks)
- **Serial Interface**
  - Standard SPI : CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI : CLK, CS#, DQ0, DQ1, WP#, HOLD#
  - Quad SPI : CLK, CS#, DQ0, DQ1, DQ2, DQ3
- **High Performance**
  - 88MHz for fast read
  - Quad I/O data transfer up to 352Mbits/s
  - 2176/2048/64/16 wrap read option
  - 2K-Byte cache for fast random read
- **Advanced Security Features**
  - Write protect all/portion of memory via software
  - Individual Block array protection
  - Lockable 16K-Byte OTP region
  - 64-Bit Unique ID for each device
- **Program/Erase/Read Speed**
  - PAGE PROGRAM time : 400μs typical (w/o ECC)
  - BLOCK ERASE time : 3ms typical
  - PAGE READ time : 120μs typical (w/o ECC)
- **Single Power Supply Voltage**
  - VCC : 1.7V~1.95V
- **Advanced Features for NAND**
  - Internal ECC option, 8 bits per 528 bytes
  - INTERNAL DATA MOVE by page
  - Promised golden block0
- **Package**
  - WSON8 8x6mm (TDFN8 8x6mm)
  - All Packages are RoHS Compliant and Halogen-free
- **Reliability**
  - 100,000 Program/Erase Cycles
  - Data Retention: 10 years (w/ ECC)

3. Packaging Type and Pin Configurations

FM25LG01BI3 is offered in a WSON8 8x6mm (TDFN8 8x6mm) package as shown in Figure 1. Package diagram and dimension are illustrated at the end of this datasheet.

Figure 1 Pad Assignments, WSON8 8x6mm (TDFN8 8x6mm)



3.1. Pin Description

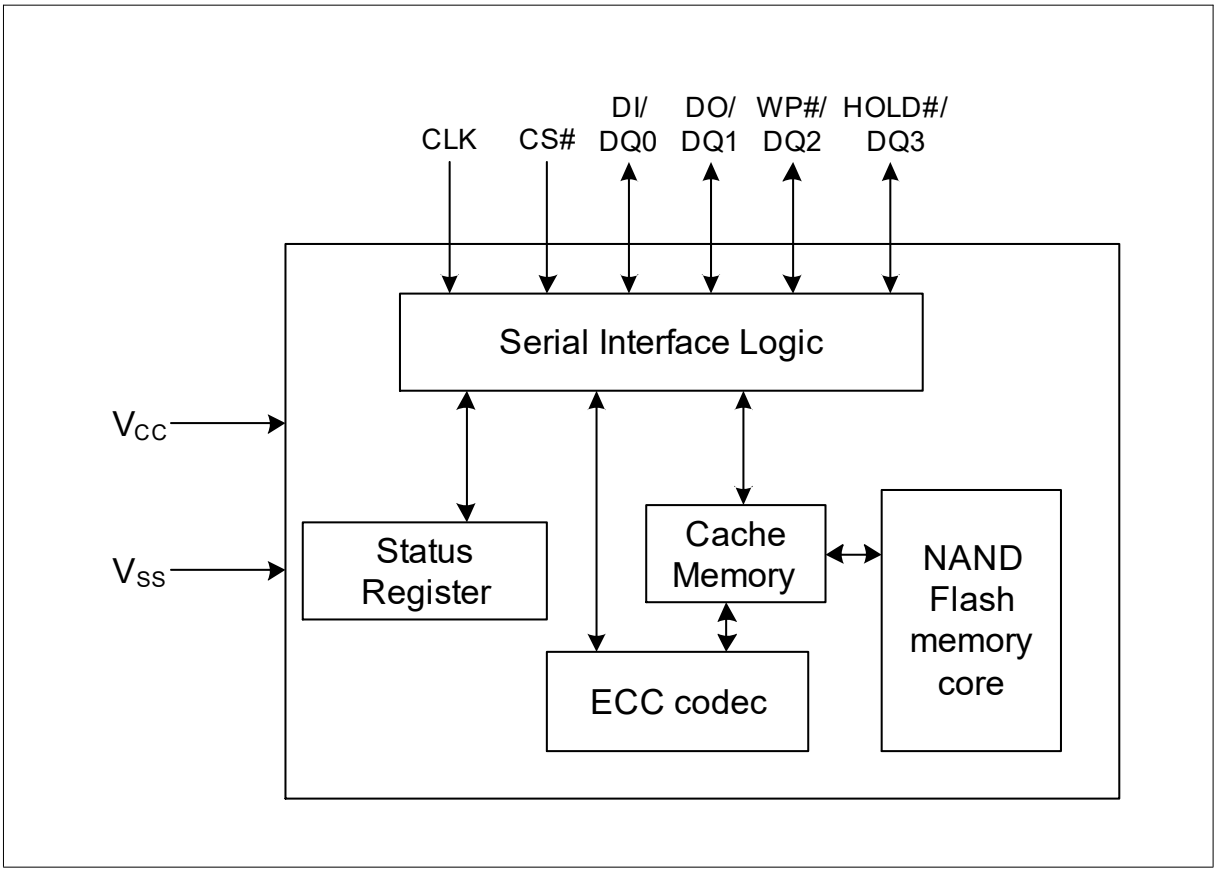
Table 1 Pin Description

PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO (DQ_1)	I/O	Data Output (Data Input Output 1)(1)
3	WP# (DQ_2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS	G	Ground
5	DI (DQ_0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	HOLD# (DQ_3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC	P	Power Supply

Notes:
1. DQ_0 and DQ_1 are used for Dual SPI instructions.
2. DQ_0 - DQ_3 are used for Quad SPI instructions.

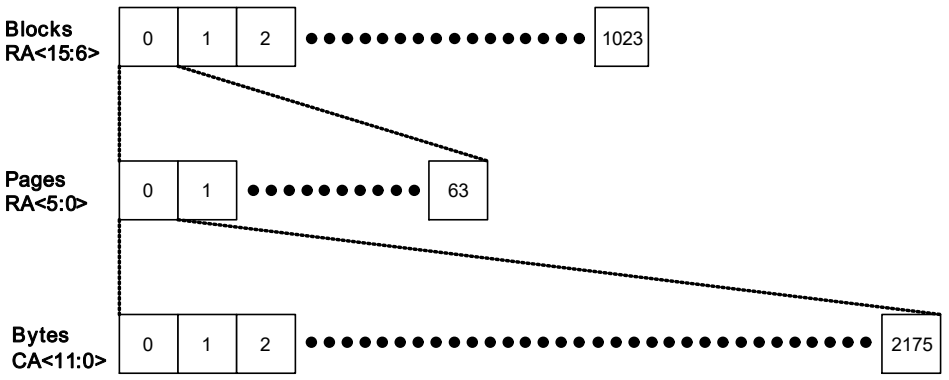
4. Block Diagram

Figure 2 SPI NAND Flash Memory Block Diagram



5. Memory Mapping

Figure 3 Memory Map



Note:

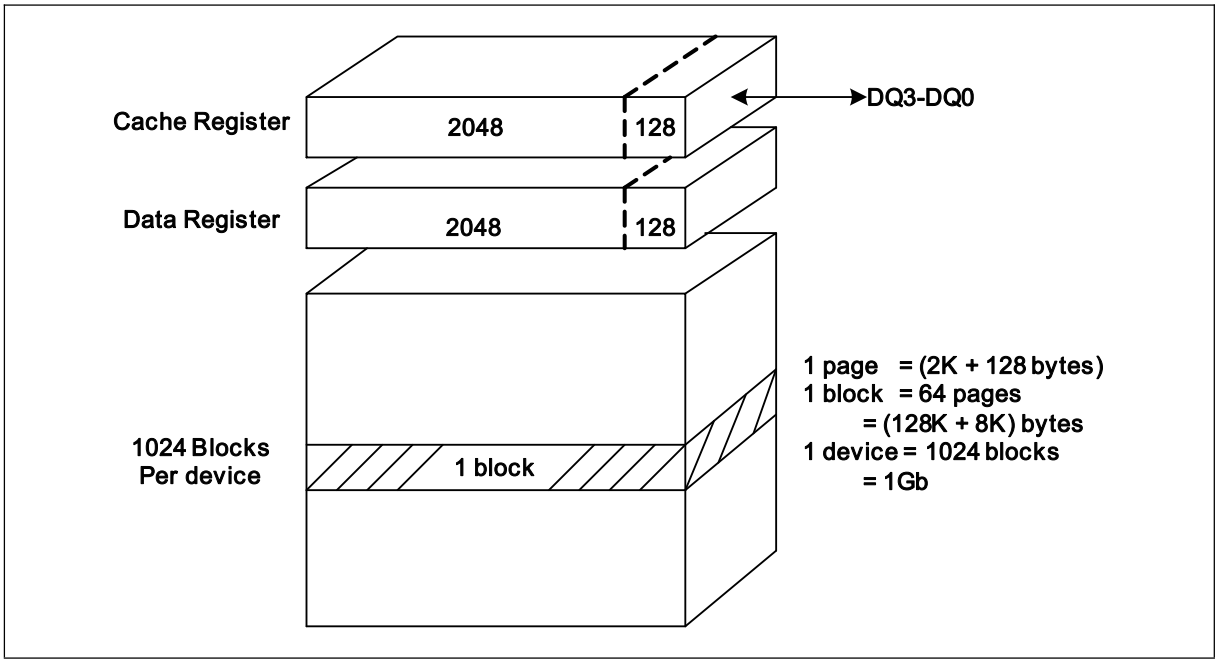
1. **CA**: Column Address. The 12-bit column address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are "out of bounds," do not exists in the device, and cannot be addressed
2. **RA**: Row Address. RA<5:0> selects a page inside a block, and RA<15:6> selects a block.

6. Array Organization

Table 2 Array Organization

Each device has	Each block has	Each page has	Unit
128M + 8M	128K + 8K	2K + 128	Bytes
1024 x 64	64	-	Pages
1024	-	-	Blocks

Figure 4 Array Organization



7. Device Operations

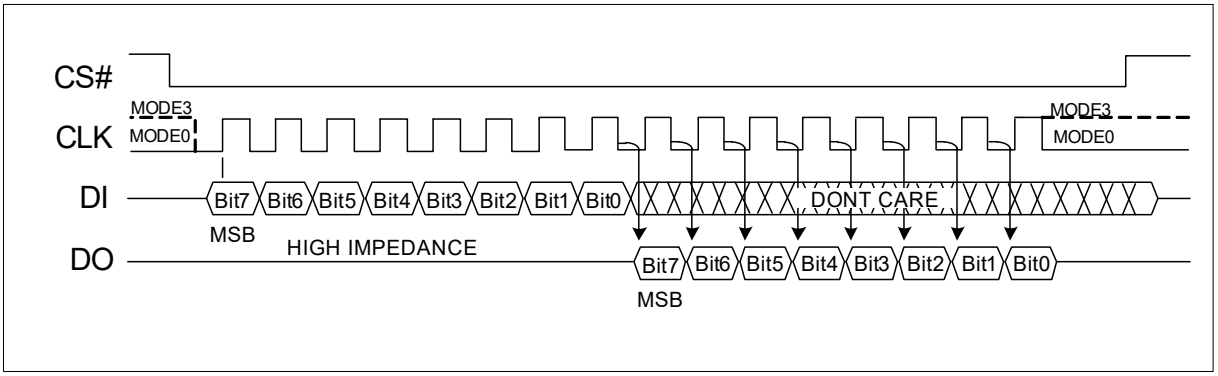
7.1. Single Data Rate (SDR)

7.1.1. Standard SPI

The FM25LG01BI3 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

Figure 5 SPI SDR Modes Supported



7.1.2. Dual SPI

The FM25LG01BI3 supports Dual SPI operation when using the x2 and dual IO instructions. These instructions allow data to be transferred to or from the device at two times the rate of ordinary Serial Flash devices. When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

7.1.3. Quad SPI

The FM25LG01BI3 supports Quad SPI operation when using the x4 and Quad IO instructions. These instructions allow data to be transferred to or from the device four times the rate of ordinary Serial Flash. When using Quad SPI instructions the DI and DO pins become bidirectional DQ_0 and DQ_1 and the WP # and HOLD# pins become DQ_2 and DQ_3 respectively. Quad SPI instructions require the Quad Enable bit (QE) to be set.

7.2. CS#

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2, DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program, read, reset or individual block lock / unlock cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

7.3. CLK

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the CLK signal. Data output changes after the falling edge of CLK.

7.4. Serial Input (DI) / DQ0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial CLK clock signal.

DI becomes DQ0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

7.5. Serial Output (DO) / DQ1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial CLK clock signal.

DO becomes DQ1 - an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

7.6. Write Protect (WP#) / DQ2

When WP# is driven Low (VIL), during a SET FEATURES command and while the BRWD bit of the Status Register is set to a 1, it is not possible to write to the Status Registers. This prevents any alteration of the Block Protect (BP2, BP1, BP0), INV and CMP bits of the Status Register. As a consequence, all the data bytes in the memory area that are protected by the Block Protect(BP2, BP1, BP0), INV and CMP bits, are also hardware protected against data modification if WP# is Low during a SET FEATURES command.

The WP# function is replaced by DQ2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

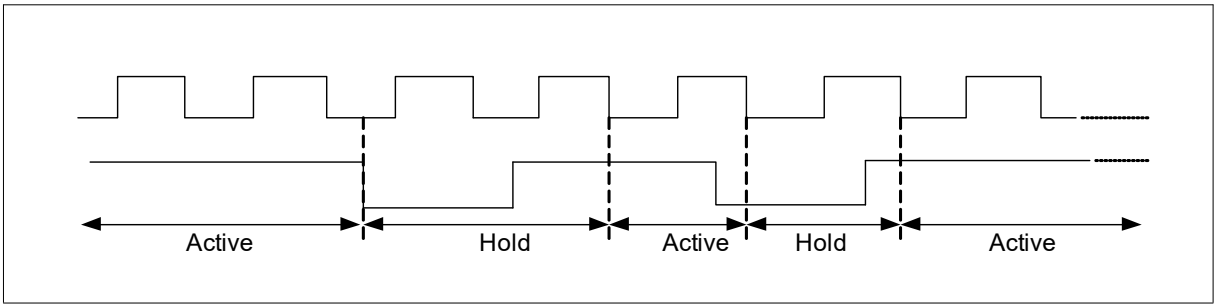
7.7. Hold (HOLD#) / DQ3

For Standard SPI and Dual SPI operations, the HOLD# signal allows the FM25LG01BI3 operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low, the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate and next data will shift out on the falling edge of CLK if HOLD# signal is already high. During a HOLD# condition, the Serial Output (DO) is high impedance, and Serial Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

The HOLD# function is not available when the Quad mode is enabled (QE =1). The Hold function is replaced by DQ3 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

Figure 6 Hold Condition Waveform



8. Command Definition

8.1. Command Set Tables

Table 3 Standard SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
WRITE ENABLE	06h					
WRITE DISABLE	04h					
GET FEATURES	0Fh	A7-A0	(D7-D0)			
SET FEATURES	1Fh	A7-A0	D7-D0			
PAGE READ	13h	A23-A16	A15-A8	A7-A0		
READ FROM CACHE	03h/0Bh	A15-A8(2)	A7-A0	dummy	(D7-D0)	wrap
READ ID	9Fh	dummy	(MID) (8)	(DID) (8)		wrap
READ UID	4Bh	dummy	dummy	dummy	dummy	(D7-D0)
PROGRAM LOAD	02h	A15-A8(6)	A7-A0	D7-D0	Next byte	Byte N
PROGRAM LOAD RANDOM DATA(9)	84h	A15-A8(6)	A7-A0	D7-D0	Next byte	Byte N
PROGRAM EXECUTE	10h	A23-A16	A15-A8	A7-A0		
BLOCK ERASE	D8h	A23-A16	A15-A8	A7-A0		
RESET	FFh					
INDIVIDUAL BLOCK LOCK	36h	A23-A16	A15-A8	A7-A0	(10)	
INDIVIDUAL BLOCK UNLOCK	39h	A23-A16	A15-A8	A7-A0	(10)	
READ BLOCK LOCK	3Dh	A23-A16	A15-A8	A7-A0	(D7-D0)	(10)
GLOBAL BLOCK LOCK	7Eh					
GLOBAL BLOCK UNLOCK	98h					

Table 4 Dual SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
READ FROM CACHE x 2	3Bh	A15-A8(2)	A7-A0	dummy	(D7-D0)x2	wrap
READ FROM CACHE DUAL IO	BBh	A15-A0(3)	dummy(4)	(D7-D0)x2		wrap

Table 5 Quad SPI Command Set

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE N
READ FROM CACHE x4	6Bh	A15-A8(2)	A7-A0	dummy	(D7-D0)x4	wrap
READ FROM CACHE QUAD IO	EBh	A15-A0(5)	(D7-D0)x4			wrap
PROGRAM LOAD x4	32h	A15-A8(6)	A7-A0	(D7-D0)x4	Next byte	Byte N
PROGRAM LOAD RANDOM DATA x4(9)	C4h/34h	A15-A8(6)	A7-A0	(D7-D0)x4	Next byte	Byte N
PROGRAM LOAD RANDOM DATA Quad IO(9)	72h	A15-A0(7)	(D7-D0)x4	Next byte		Byte N

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 DQ pins.
2. The x8 clock = wrap<3:0>, A11-A8
3. The x8 clock = wrap<3:0>, A11-A0
4. The x8 clock = dummy<7:0>, D7-D0
5. The x8 clock = wrap<3:0>, A11-A0, dummy<7:0>, D7-D0

6. The x8 clock = dummy<3:0>, A11-A8
7. The x8 clock = dummy<3:0>, A11-A0, D7-D0, D7-D0
8. MID is Manufacture ID (A1h for FMSH), DID is Device ID (B1h for current device)
9. Only available in INTERNAL DATA MOVE operation
10. A<23:22>=00, A<21:12> is RA<15:6>, A<11:0> is dummy bits

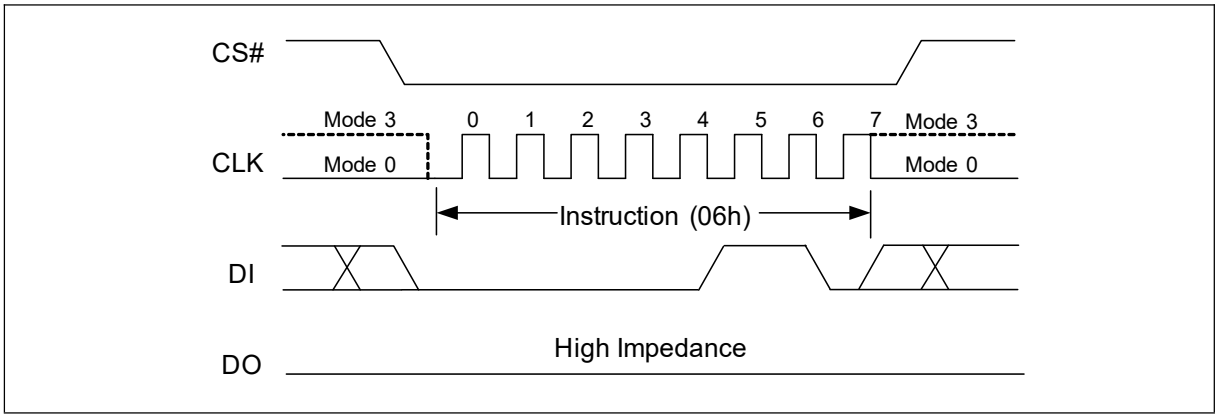
8.2. WRITE operation

8.2.1. WRITE ENABLE (WREN) (06h)

The WRITE ENABLE (WREN) command sets the WEL bit in the status register to 1. The WEL bit must be set prior to following operations that changes the contents of the memory array:

- PAGE PROGRAM
- OTP PROGRAM
- OTP LOCK
- BLOCK ERASE

Figure 7 WRITE ENABLE (06h) Timing

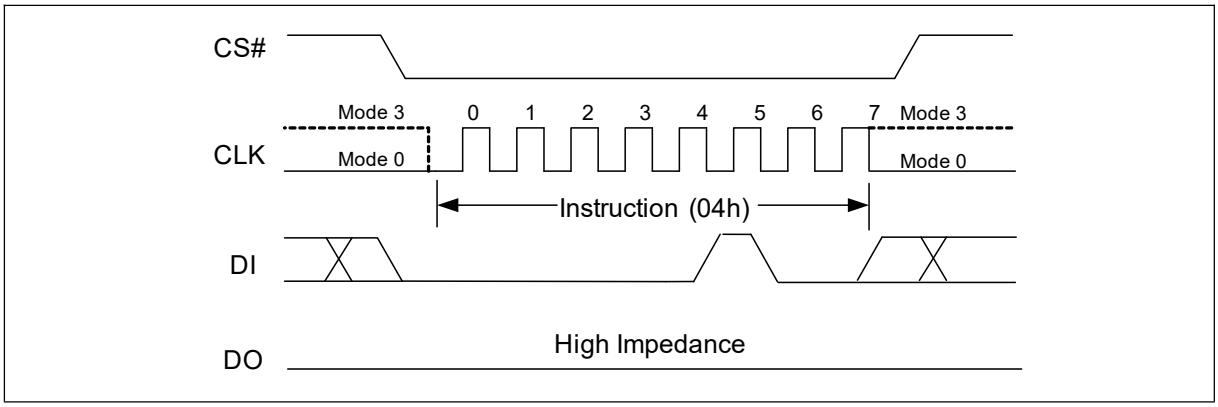


8.2.2. WRITE DISABLE (WRDI) (04h)

The WRITE DISABLE (WRDI) command resets the WEL bit in the status register to 0. The WEL bit is automatically reset after Power-up and upon completion of the following operations:

- PAGE PROGRAM
- OTP PROGRAM
- OTP LOCK
- BLOCK ERASE

Figure 8 WRITE DISABLE (04h) Timing



8.3. Feature Operation

8.3.1. GET FEATURES (0Fh) and SET FEATURES (1Fh)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific bits in feature address A0h and B0h (shown the following table). The status register is mostly read, except WEL, which is writable bit with the WREN (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table 6 Features Settings

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
ECC Config	90h	Reserved	Reserved	Reserved	ECC_EN	Reserved	Reserved	Reserved	Reserved
Block Lock	A0h	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0h	OTP_PRT	OTP_EN	WPS	Reserved	Reserved	Reserved	Reserved	QE
Status	C0h	Reserved	ECCS2	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP

Notes:
1. If BRWD is enabled and WP# is low, then the block lock register (BP2-BP0, INV and CMP) cannot be changed.
2. If QE is enabled, the quad IO operations can be executed.
3. All the reserved bits must be held low when the feature is set.
4. The OTP_PRT is non-volatile, whereas other bits are volatile.

Figure 9 GET FEATURES (0Fh) Timing

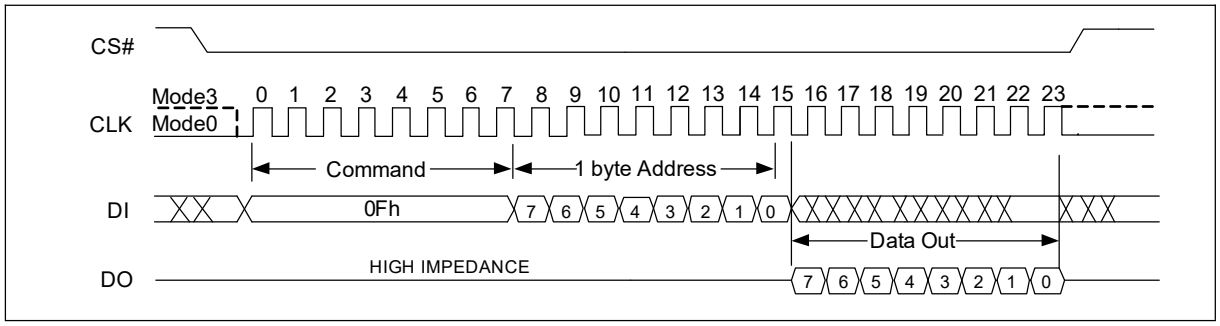
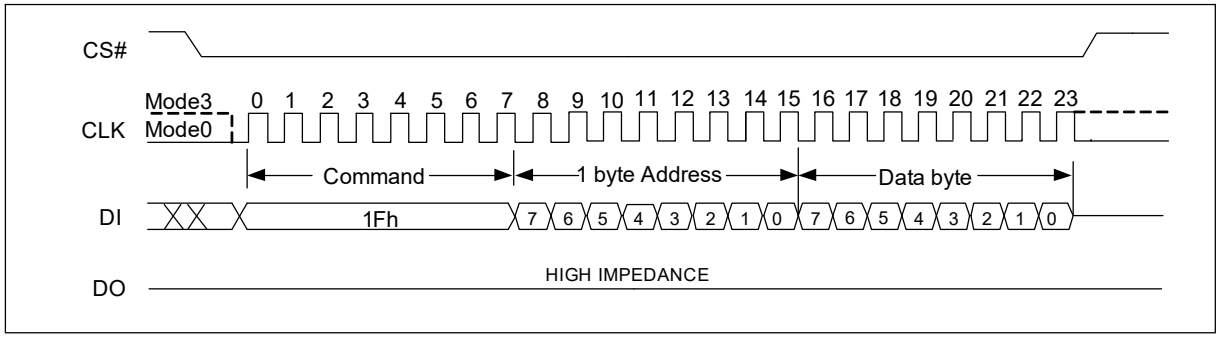


Figure 10 SET FEATURES (1Fh) Timing



8.4. READ Operation

8.4.1. PAGE READ

The device supports "Power-on Read" function. After power up, the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the 1st page of 1st block data from the cache buffer. The cache data is promised correctly with internal ECC on default.

The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is follows:

- 13h (PAGE READ TO CACHE)
- 0Fh (GET FEATURES command to read the status)
- 0Bh or 03h (READ FROM CACHE)
- READ FROM CACHE Operation
  - 3Bh (READ FROM CACHE x2)
  - 6Bh (READ FROM CACHE x4)
  - BBh (READ FROM CACHE DUAL IO)
  - EBh (READ FROM CACHE QUAD IO)

The PAGE READ command requires a 24-bit address consisting of 8 dummy bits followed by a 16-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for t_{RD} time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation (refer to the Status Register section). Following a status of successful completion, the READ FROM CACHE (03h/0Bh/3Bh/6Bh/BBh/EBh) command must be issued in order to read the data out of the cache.

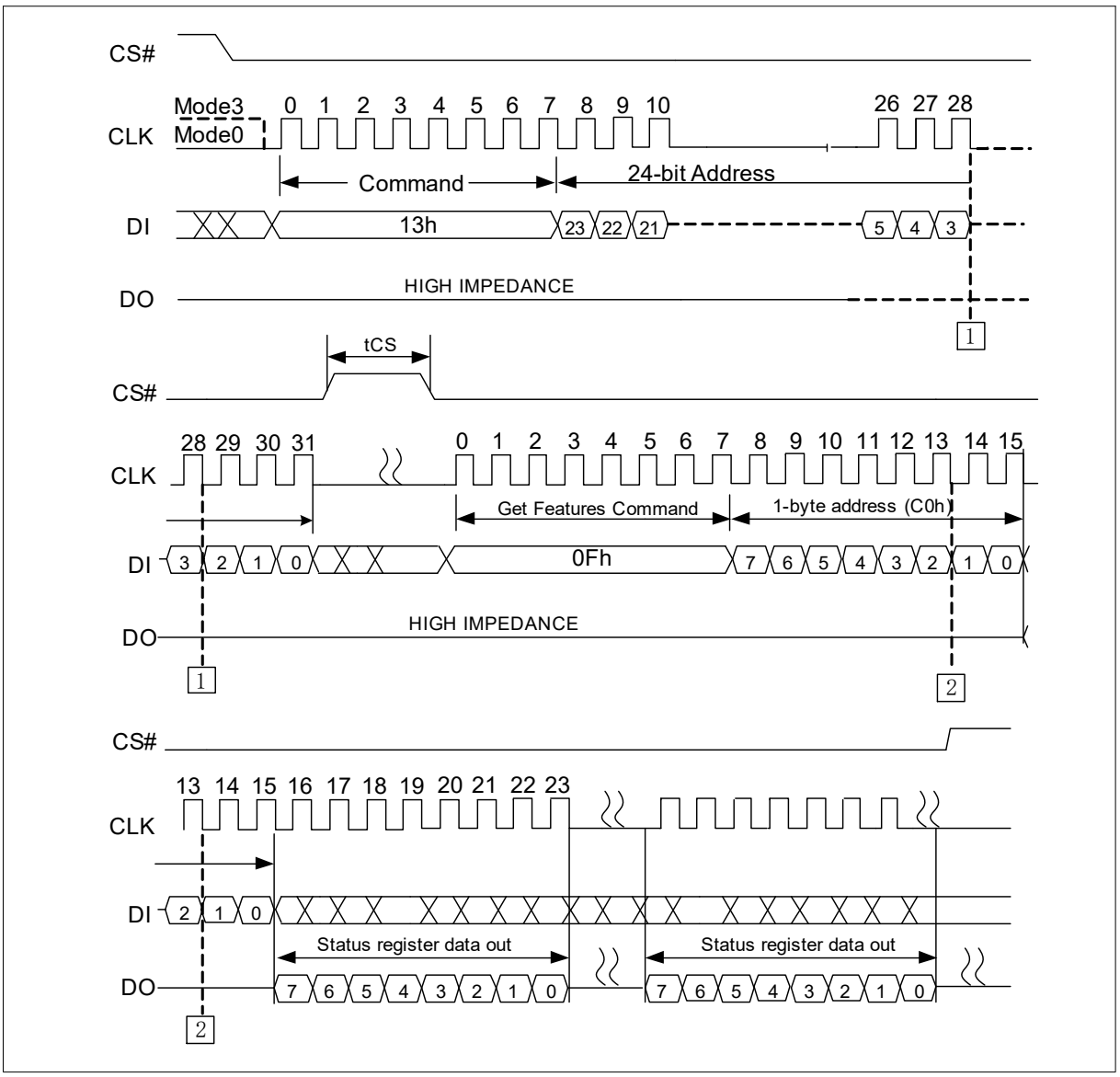
The READ FROM CACHE command requires 4 wrap mode configure bits, followed by a 12-bit column address for the starting byte address. The starting byte address must be in 0 to 2175. After the end of the cache register is reached, the data wraps around the beginning boundary automatically until CS# is pulled high to terminate this operation.

Table 7 Wrap Configure Bit Table

Wrap<3:0>	Wrap Length (byte)
00xx	2176
01xx	2048
10xx	64
11xx	16

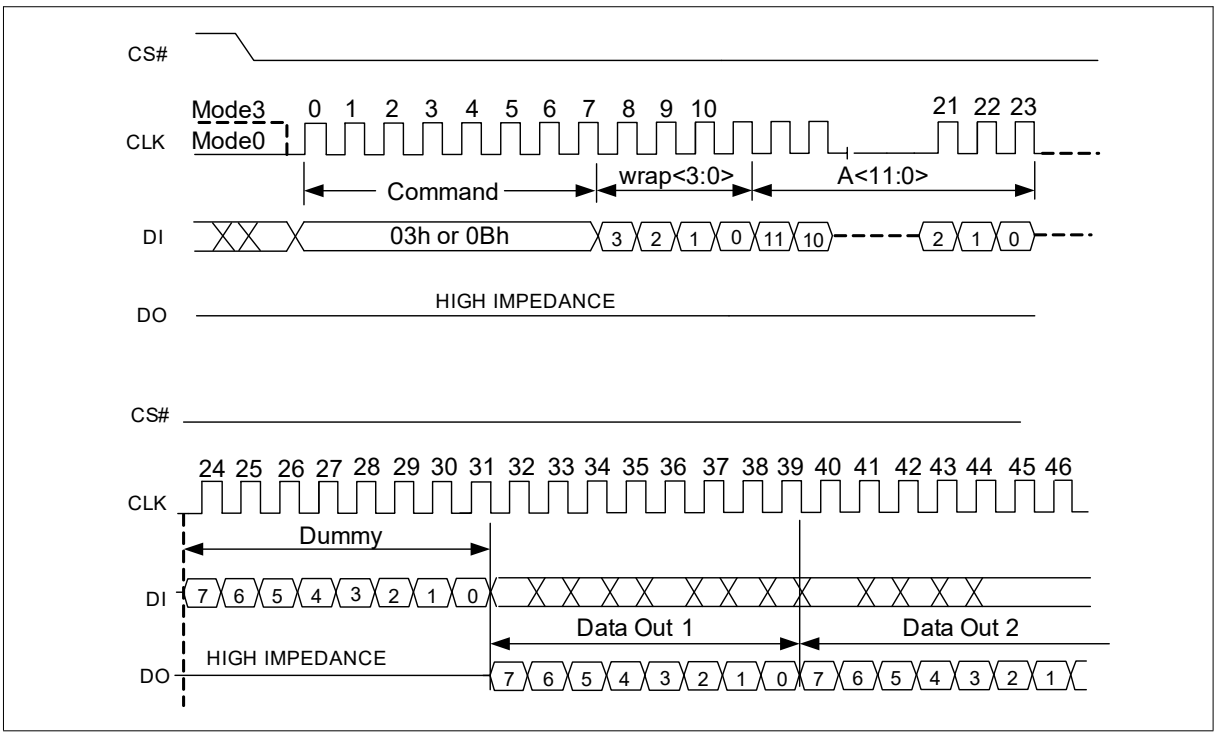
8.4.1. PAGE READ TO CACHE (13h)

Figure 11 PAGE READ TO CACHE (13h) Timing



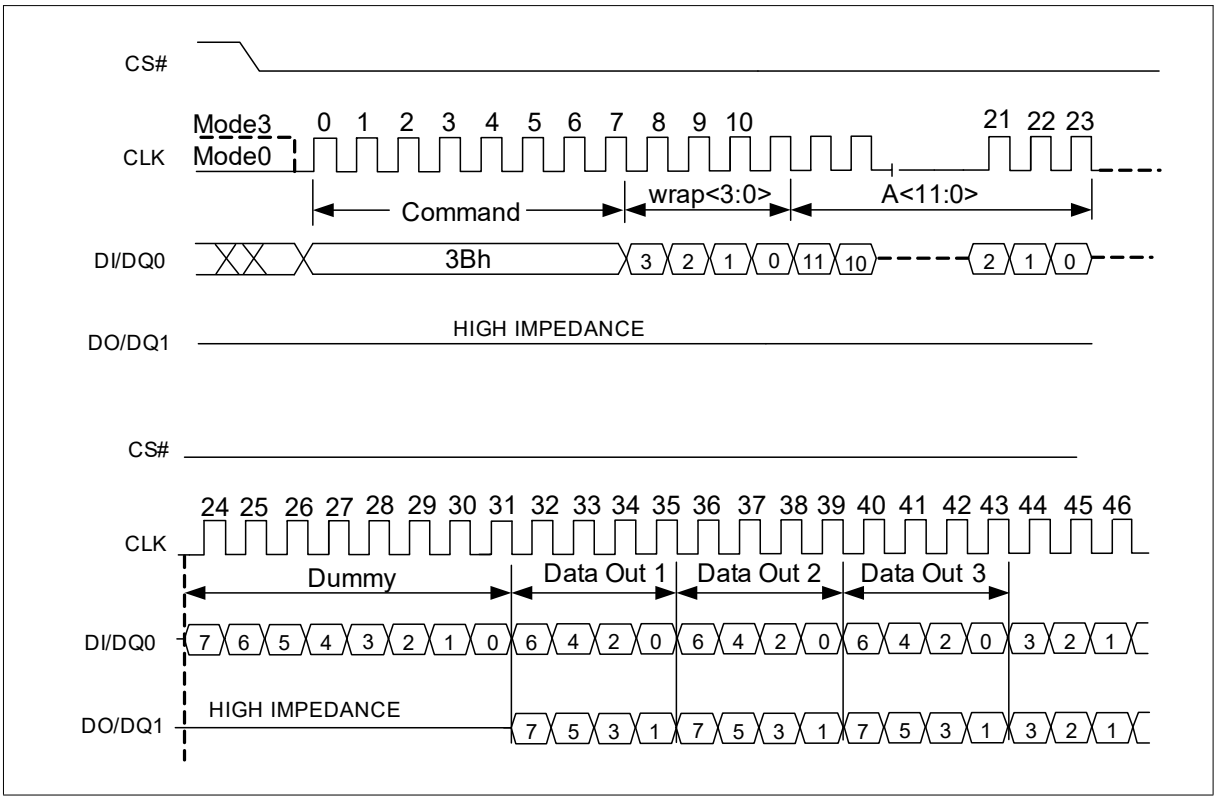
8.4.2. READ FROM CACHE (03h/0Bh)

Figure 12 READ FROM CACHE (03h / 0Bh) Timing



8.4.3. READ FROM CACHE x2 (3Bh)

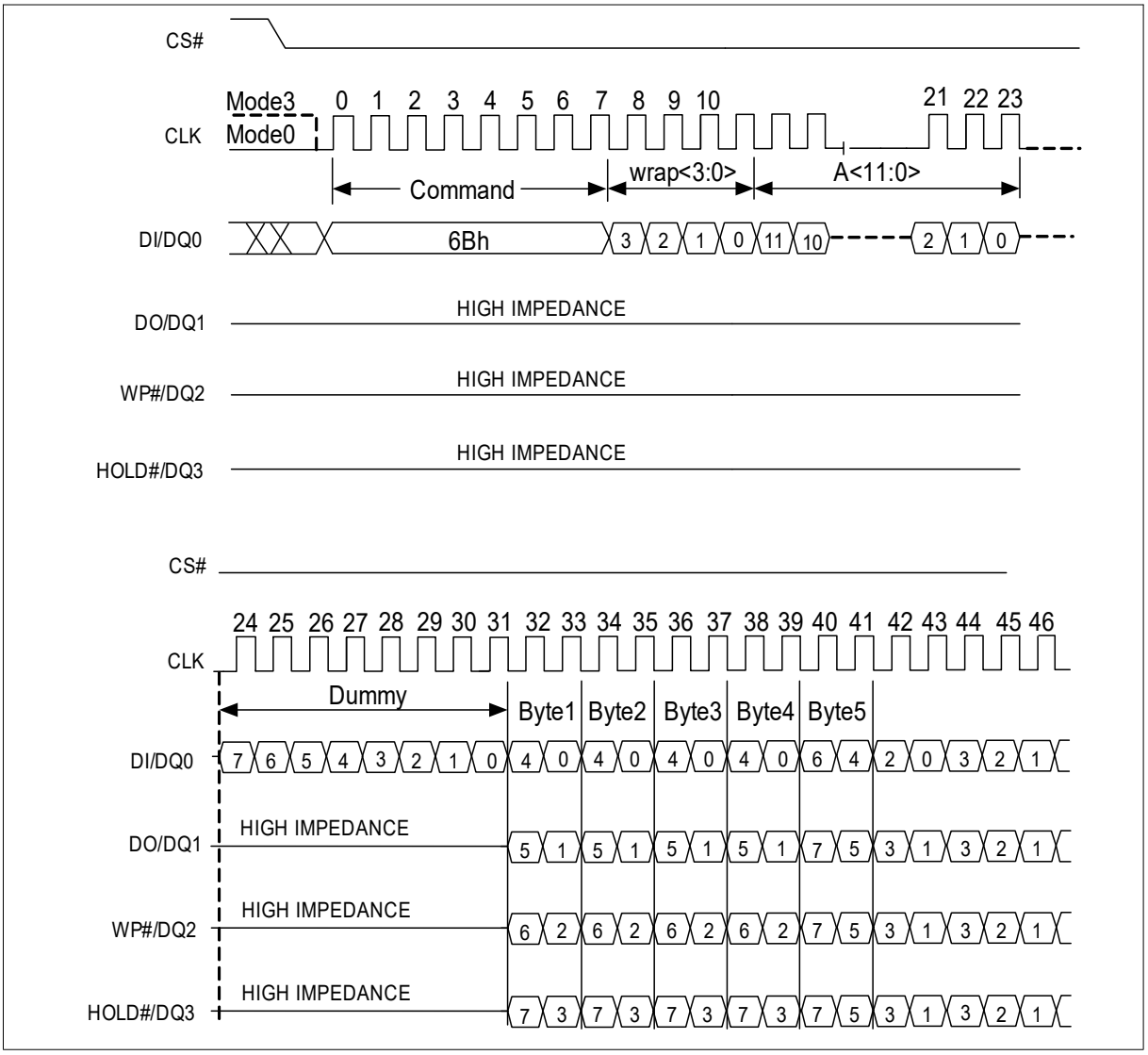
Figure 13 READ FROM CACHE x2 (3Bh) Timing



8.4.4. READ FROM CACHE x4 (6Bh)

The Quad Enable bit (QE) of feature (B0h[0]) must be set to enable the READ FROM CACHE x4 command.

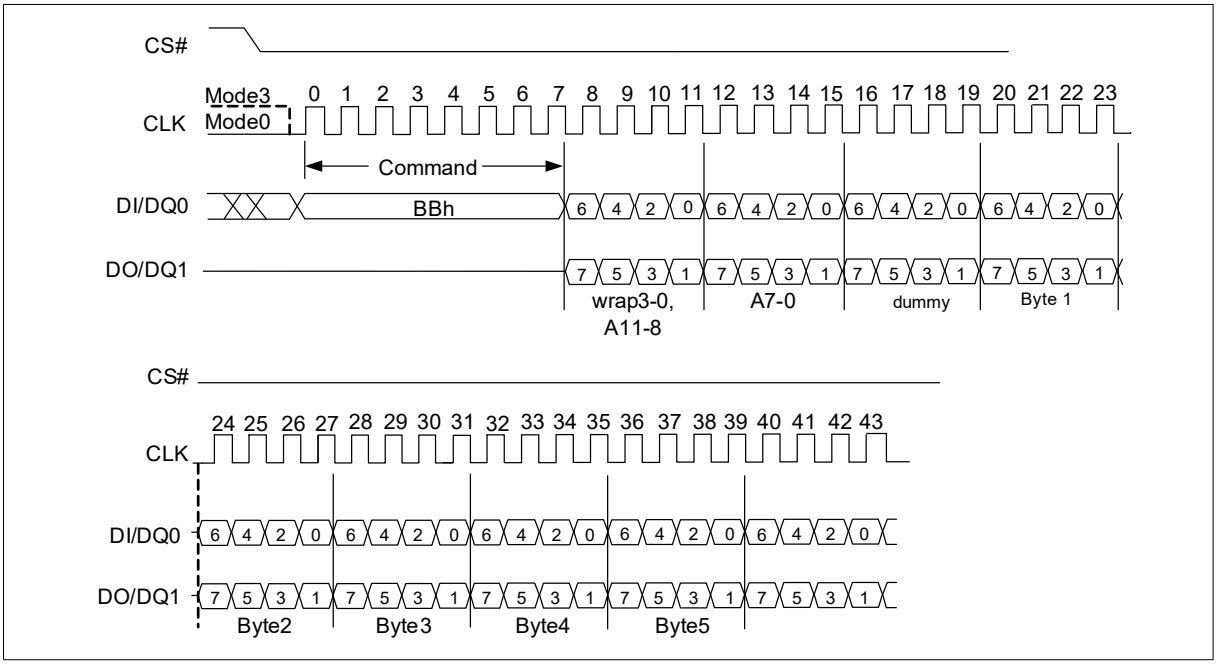
Figure 14 READ FROM CACHE x4 (6Bh) Timing



8.4.5. READ FROM CACHE DUAL IO (BBh)

The READ FROM CACHE DUAL IO command is similar to the READ FROM CACHE x2 command except that wrap bits, 12-bit column address and dummy bits are input through two pins DQ_0, DQ_1.

Figure 15 READ FROM CACHE DUAL IO (BBh) Timing

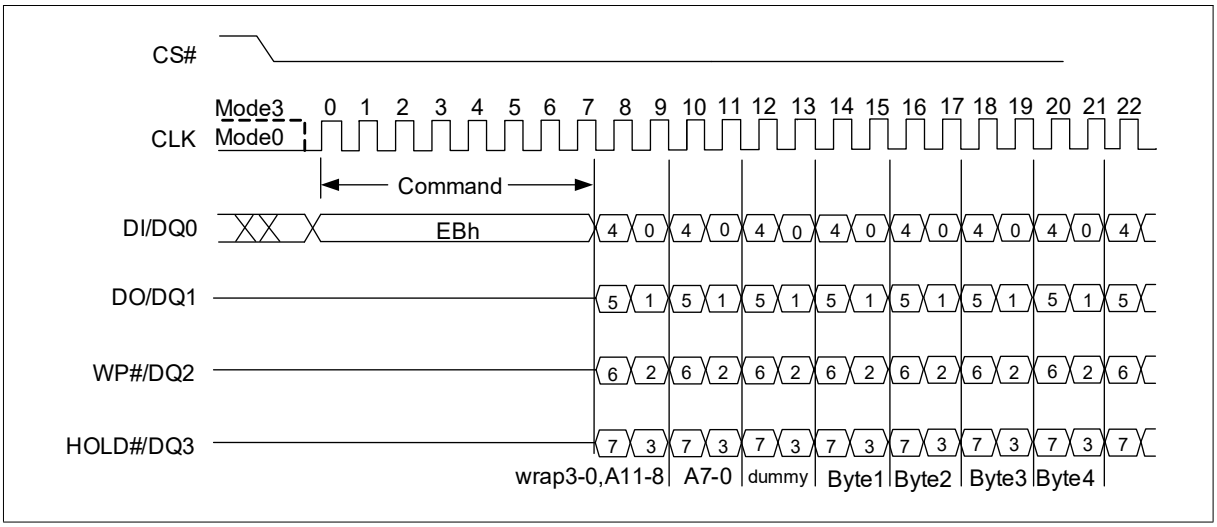


8.4.6. READ FROM CACHE QUAD IO (EBh)

The READ FROM CACHE QUAD IO command is similar to the READ FROM CACHE x4 command except that wrap bits, 12-bit column address and dummy bits are input through four pins DQ_0, DQ_1, DQ_2 and DQ_3.

The Quad Enable bit (QE) of feature (B0h[0]) must be set to enable the READ FROM CACHE QUAD IO command.

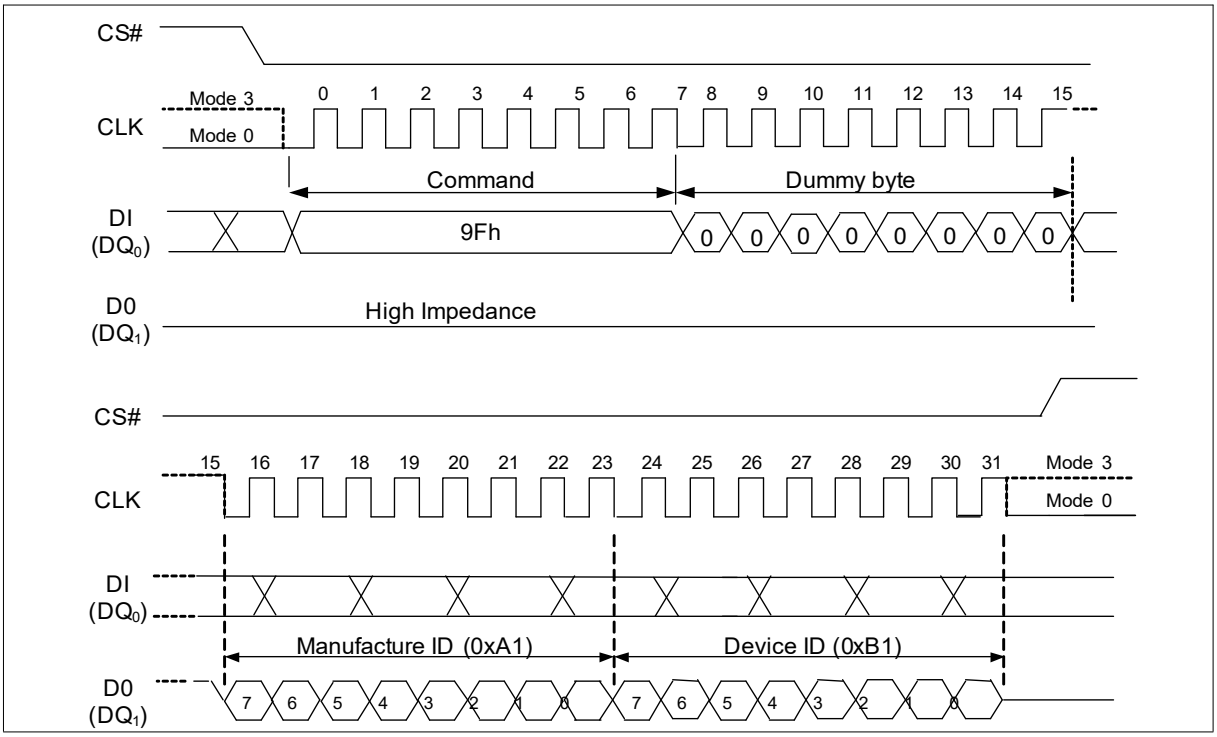
Figure 16 READ FROM CACHE QUAD IO (EBh) Timing



8.4.7. READ ID (9Fh)

The READ ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The READ ID command reads a 2-byte data (see below) that includes the Manufacturer ID and the device configuration.

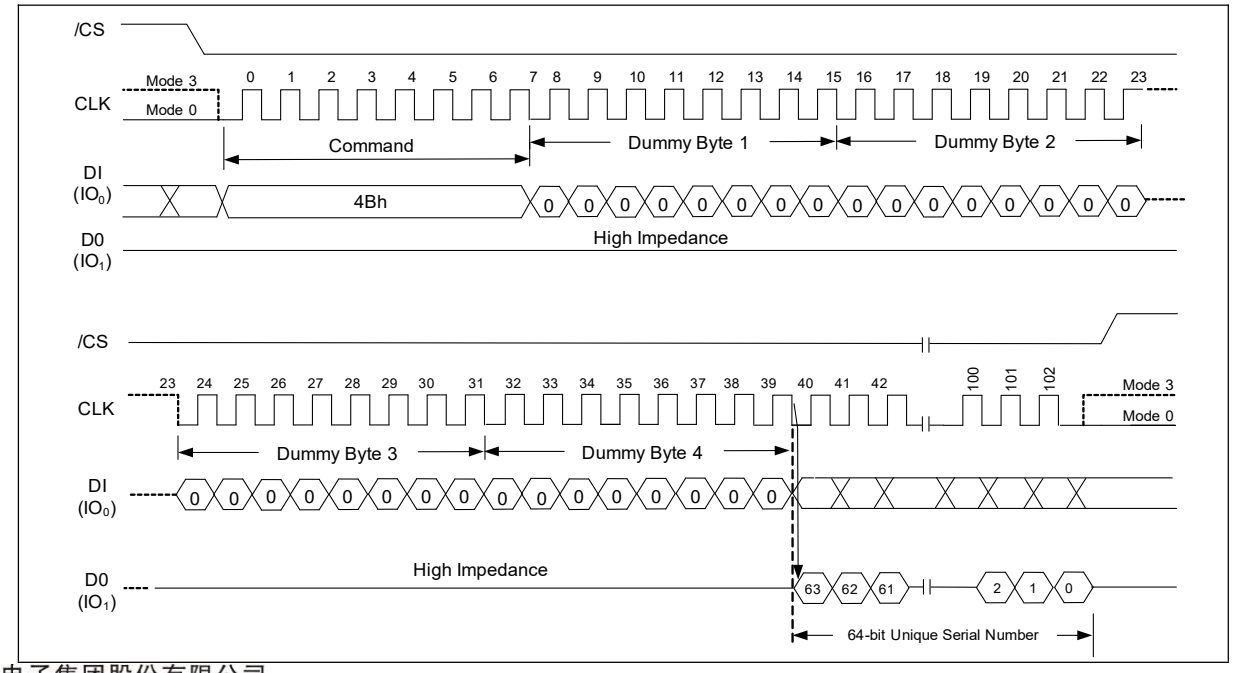
Figure 17 READ ID (9Fh) Timing



8.4.8. READ UID (4Bh)

The READ UID instruction accesses a factory-set read-only 64-bit number that is unique to each FM25LG01BI3 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system.

Figure 18 READ UID (4Bh) Timing



8.5. PROGRAM Operation

The PAGE PROGRAM operation sequence programs 1 byte to 2176 bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

The 1st step is to issue a PROGRAM LOAD (02H/32H) command. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register which is 2176 bytes long. If more than 2176 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure 19 and Figure 20 show the PROGRAM LOAD operation.

The 2nd step, prior to performing the PROGRAM EXECUTE operation, is to issue a WRITE ENABLE (06H) command. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

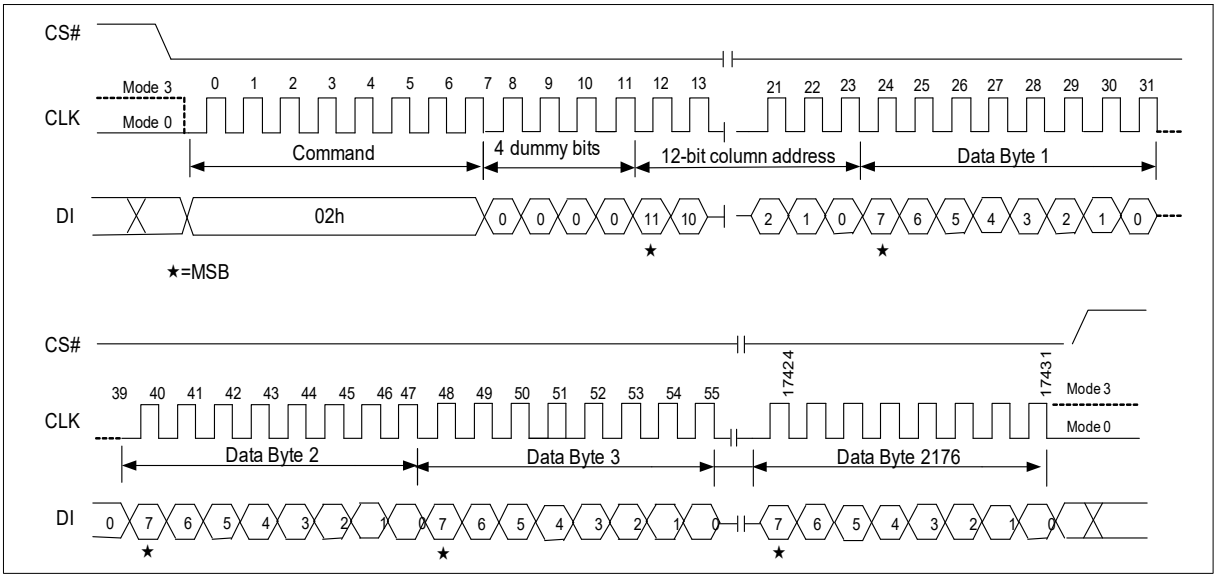
The 3rd step is to issue a PROGRAM EXECUTE (10h) command to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address (8 dummy bits and a 16-bit page/block address). After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for t_{PROG} time. This operation is shown in Figure 21.

During this busy time, the status register can be polled to monitor the status of the operation (refer to the Status Register section). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Note: The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. In addition, pages must be sequentially programmed within a block.

8.5.1. PROGRAM LOAD (02h)

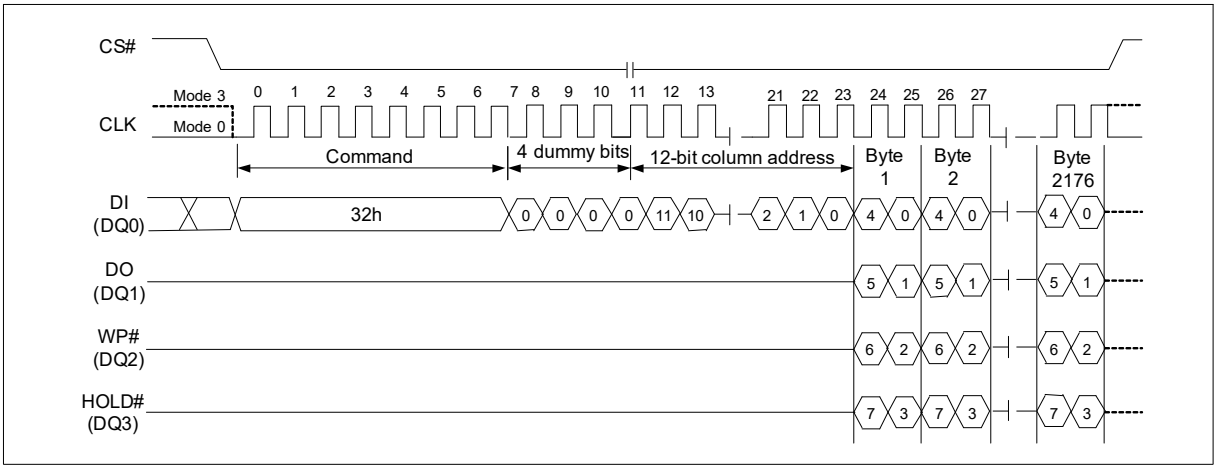
Figure 19 PROGRAM LOAD (02h) Timing



8.5.2. PROGRAM LOAD x4 (32h)

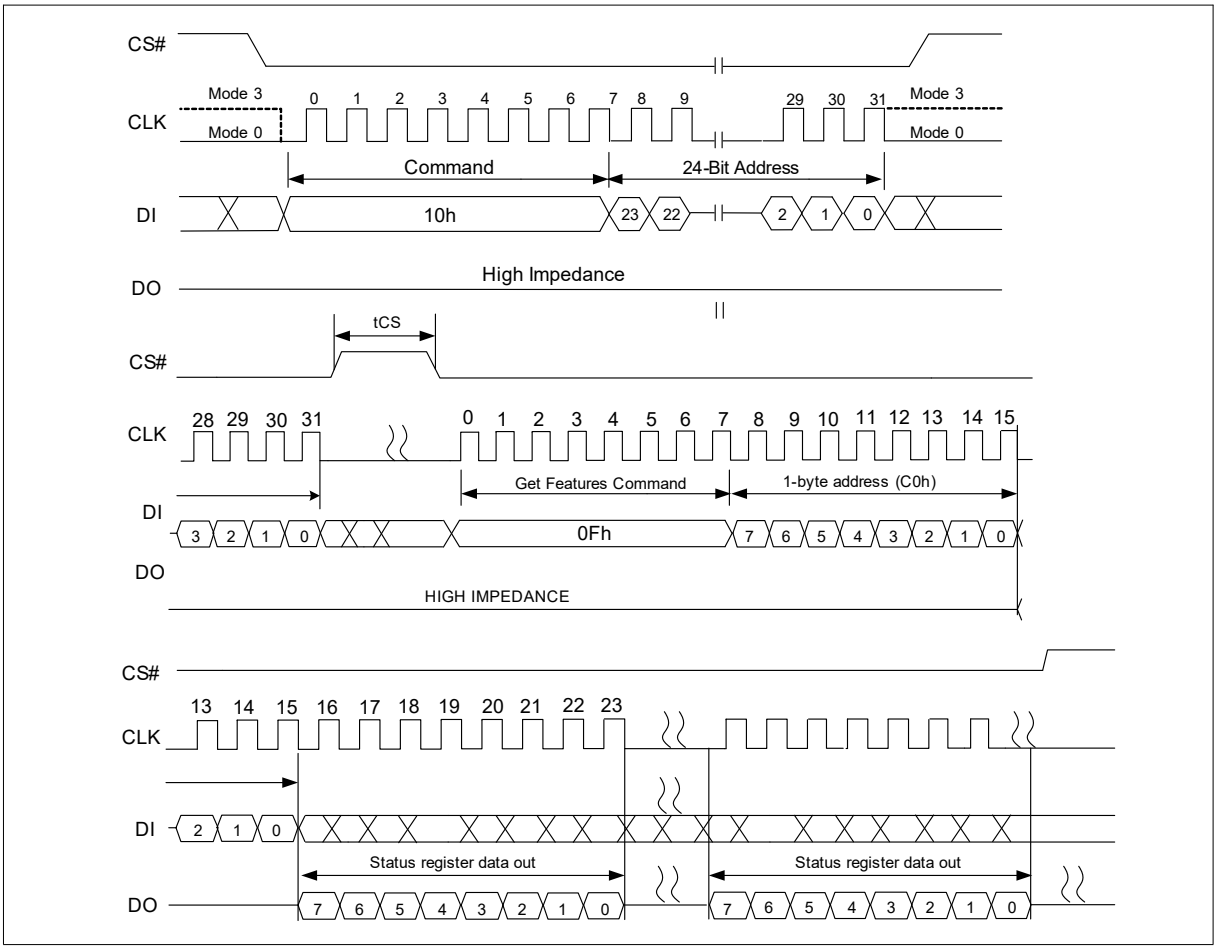
The PROGRAM LOAD x4 command (32H) is similar to the PROGRAM LOAD command (02H) but with the capability to input the data bytes by four pins: DQ0, DQ1, DQ2, and DQ3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0h[0]) must be set to enable the PROGRAM LOAD x4 command.

Figure 20 PROGRAM LOAD x4 (32h) Timing



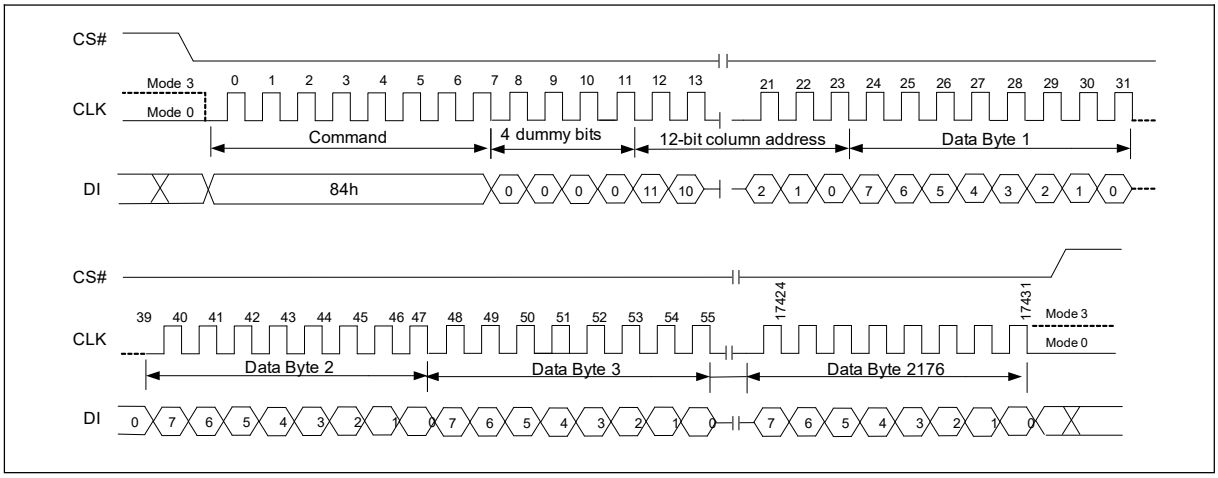
8.5.3. PROGRAM EXECUTE (PE) (10h)

Figure 21 PROGRAM EXECUTE (10h) Timing



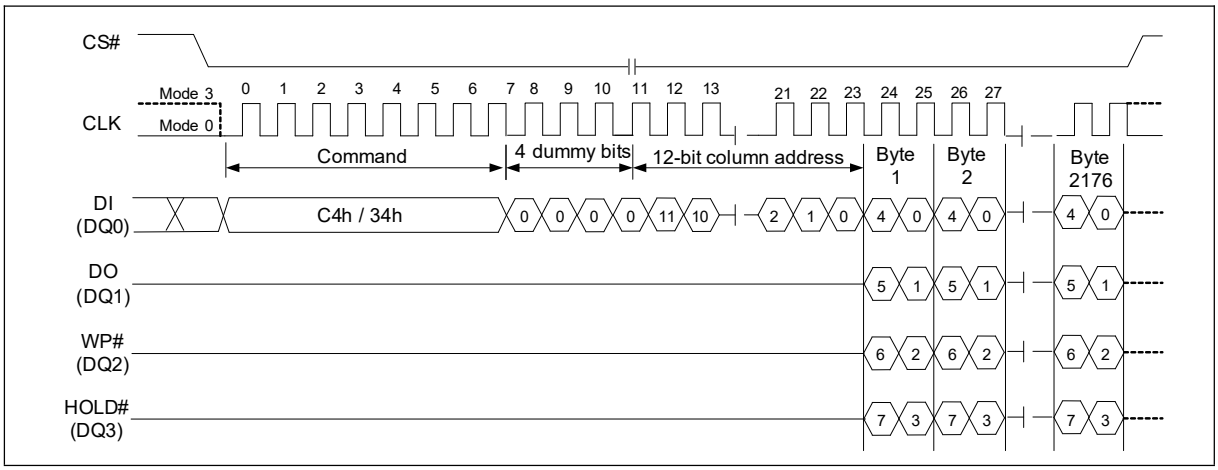
8.5.4. PROGRAM LOAD RANDOM DATA (84h)

Figure 22 PROGRAM LOAD RANDOM DATA (84h) Timing



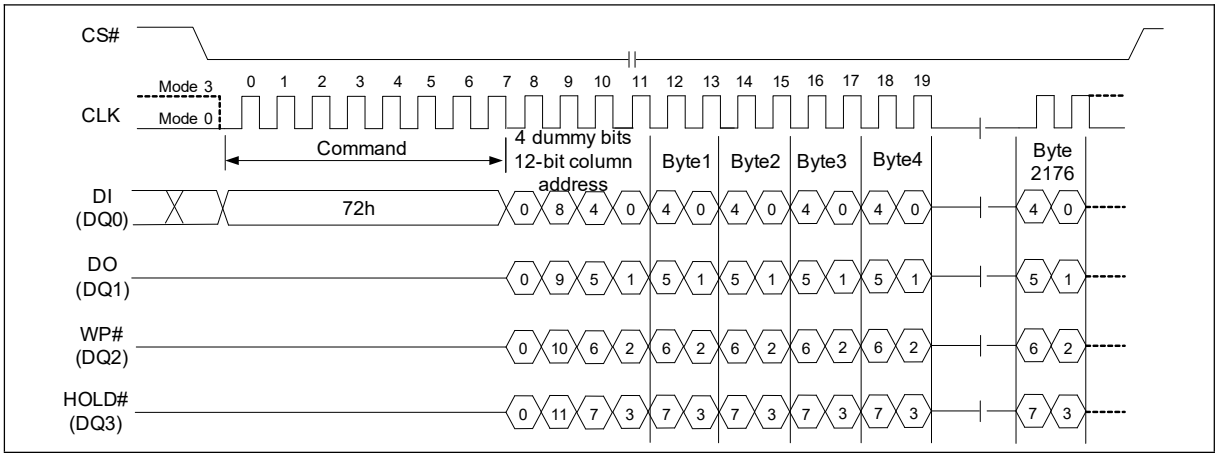
8.5.5. PROGRAM LOAD RANDOM DATA x4 (C4h/34h)

Figure 23 PROGRAM LOAD RANDOM DATA x4 (C4h/34h) Timing



8.5.6. PROGRAM LOAD RANDOM DATA Quad IO (72h)

Figure 24 PROGRAM LOAD RANDOM DATA Quad IO (72h) Timing



8.5.7. INTERNAL DATA MOVE

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

- 13H (PAGE READ TO CACHE)
- 84H/C4H/34H/72H (PROGRAM LOAD RANDOM DATA : Optional)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/C4H/34H/72H) command can be issued, if user wants to update bytes of data in the page. This command consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address. New data is loaded in the 12-bit column address. If the RANDOM DATA is not sequential, another PROGRAM LOAD RANDOM DATA (84H/C4H/34H/72H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and then a PROGRAM EXECUTE (10H) command can be issued to start the programming operation.

8.6. ERASE Operation

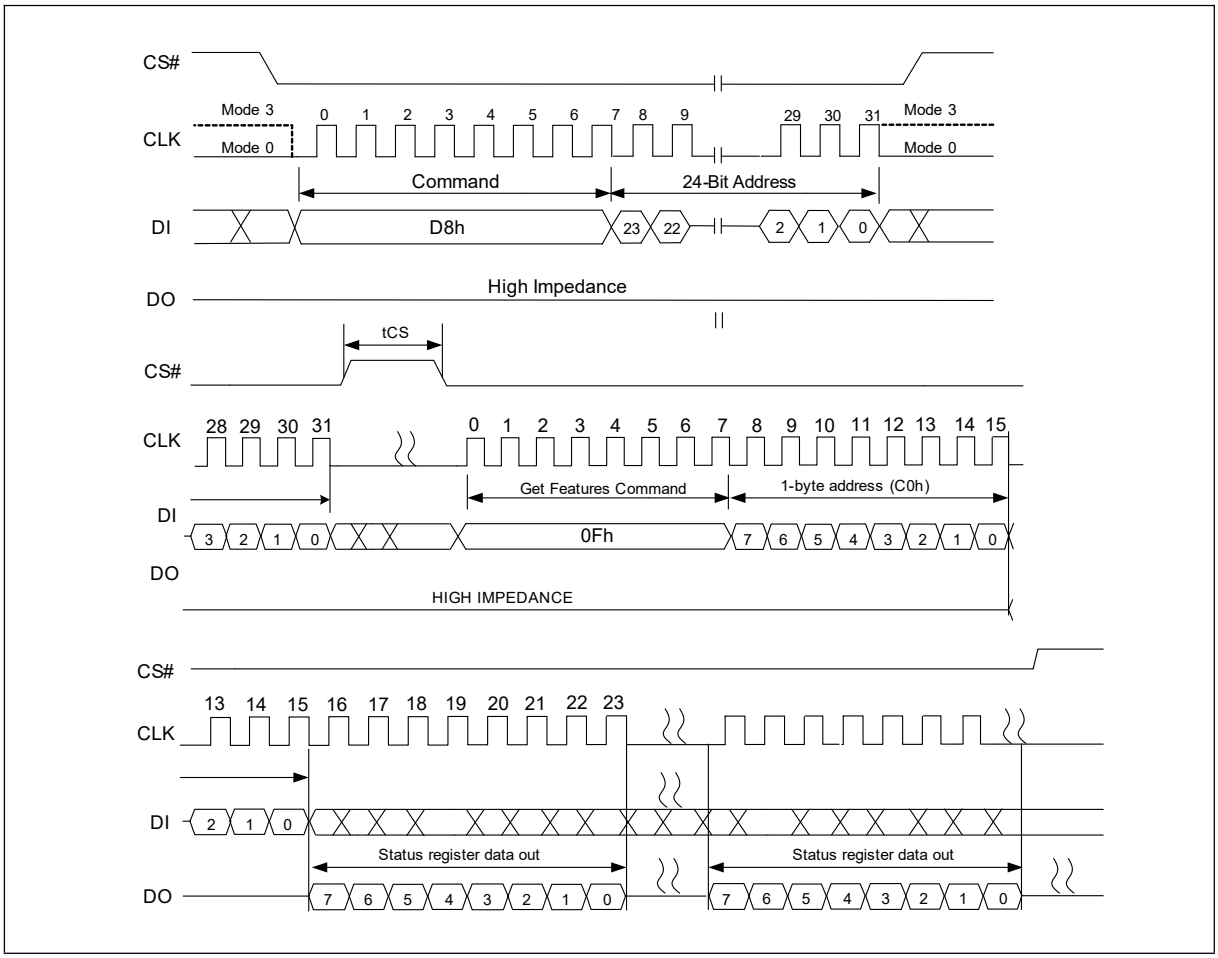
8.6.1. BLOCK ERASE (D8h)

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2176 bytes per page (2048 + 128 bytes). Each block is 136 Kbytes. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENBALE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of 8 dummy bits followed by a 16-bit row address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for t_{ERS} time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation (refer to the Status Register section).

Figure 25 BLOCK ERASE (D8h) Timing

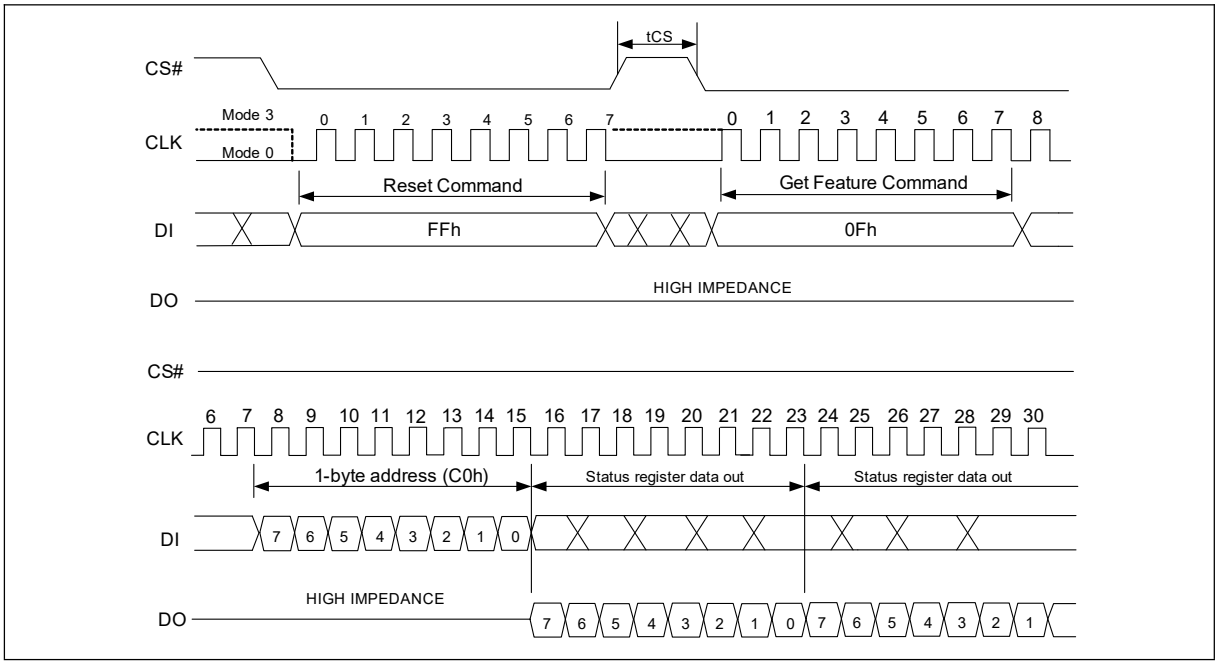


8.7. RESET Operation

The RESET (FFh) command stops all operations. For example, in case of a program or erase or read operation, the reset command can make the device enter the idle state.

8.7.1. RESET (FFh)

Figure 26 RESET (FFh) Timing



8.8. Write Protection

The WPS feature (B0h[5]) is used to select block protection method. The default value after power on reset is 0.

If WPS=0, the write protection will be determined by the combination of CMP, INV, BP[2:0] bits in the Block Lock Register (A0h).

Table 8 Block Lock Register Block Protect Bits (WPS=0)

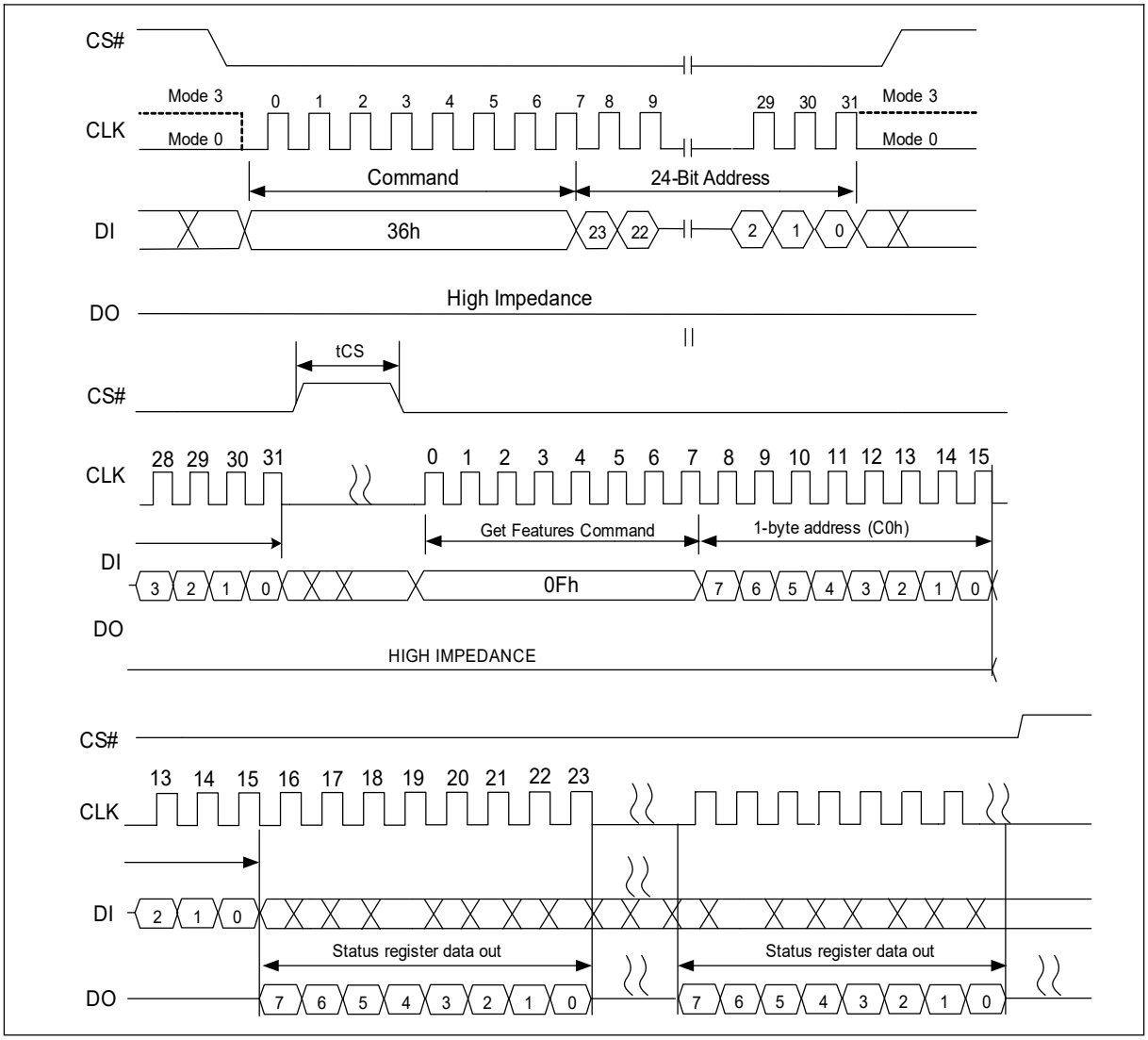
CMP	INV	BP2	BP1	BP0	Protected Row Address	Protected Rows
x	x	0	0	0	None	None
0	0	0	0	1	0FC00h~0FFFFh	Upper 1/64
0	0	0	1	0	0F800h~0FFFFh	Upper 1/32
0	0	0	1	1	0F000h~0FFFFh	Upper 1/16
0	0	1	0	0	0E000h~0FFFFh	Upper 1/8
0	0	1	0	1	0C000h~0FFFFh	Upper 1/4
0	0	1	1	0	08000h~0FFFFh	Upper 1/2
x	x	1	1	1	All (default)	All (default)
0	1	0	0	1	00000h~003FFh	Lower 1/64
0	1	0	1	0	00000h~007FFh	Lower 1/32
0	1	0	1	1	00000h~00FFFh	Lower 1/16
0	1	1	0	0	00000h~01FFFh	Lower 1/8
0	1	1	0	1	00000h~03FFFh	Lower 1/4
0	1	1	1	0	00000h~07FFFh	Lower 1/2
1	0	0	0	1	00000h~0FBFFh	Lower 63/64
1	0	0	1	0	00000h~0F7FFh	Lower 31/32
1	0	0	1	1	00000h~0EFFFh	Lower 15/16
1	0	1	0	0	00000h~0DFFFh	Lower 7/8
1	0	1	0	1	00000h~0BFFFh	Lower 3/4
1	0	1	1	0	00000h~0003Fh	Block0
1	1	0	0	1	00400h~0FFFFh	Upper 63/64
1	1	0	1	0	00800h~0FFFFh	Upper 31/32
1	1	0	1	1	01000h~0FFFFh	Upper 15/16
1	1	1	0	0	02000h~0FFFFh	Upper 7/8
1	1	1	0	1	04000h~0FFFFh	Upper 3/4
1	1	1	1	0	00000h~0003Fh	Block0

If WPS=1, the INDIVIDUAL BLOCK LOCK is enabled. The INDIVIDUAL BLOCK LOCK provides an alternative way to protect the memory array from adverse Erase/Program. The INDIVIDUAL BLOCK LOCK bits are volatile bits. The default values after power up or after Reset are 1, so the entire memory array is being protected.

8.8.1. INDIVIDUAL BLOCK LOCK (36h)

The INDIVIDUAL BLOCK LOCK command requires a 24-bit address consisting of 2-bit '0' followed by a 10-bit block address (RA<5:0> is don't care) and 12 dummy bits. After the addresses are registered, the device starts setting the corresponding INDIVIDUAL BLOCK LOCK bit, and is busy for t_{LCK} time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation.

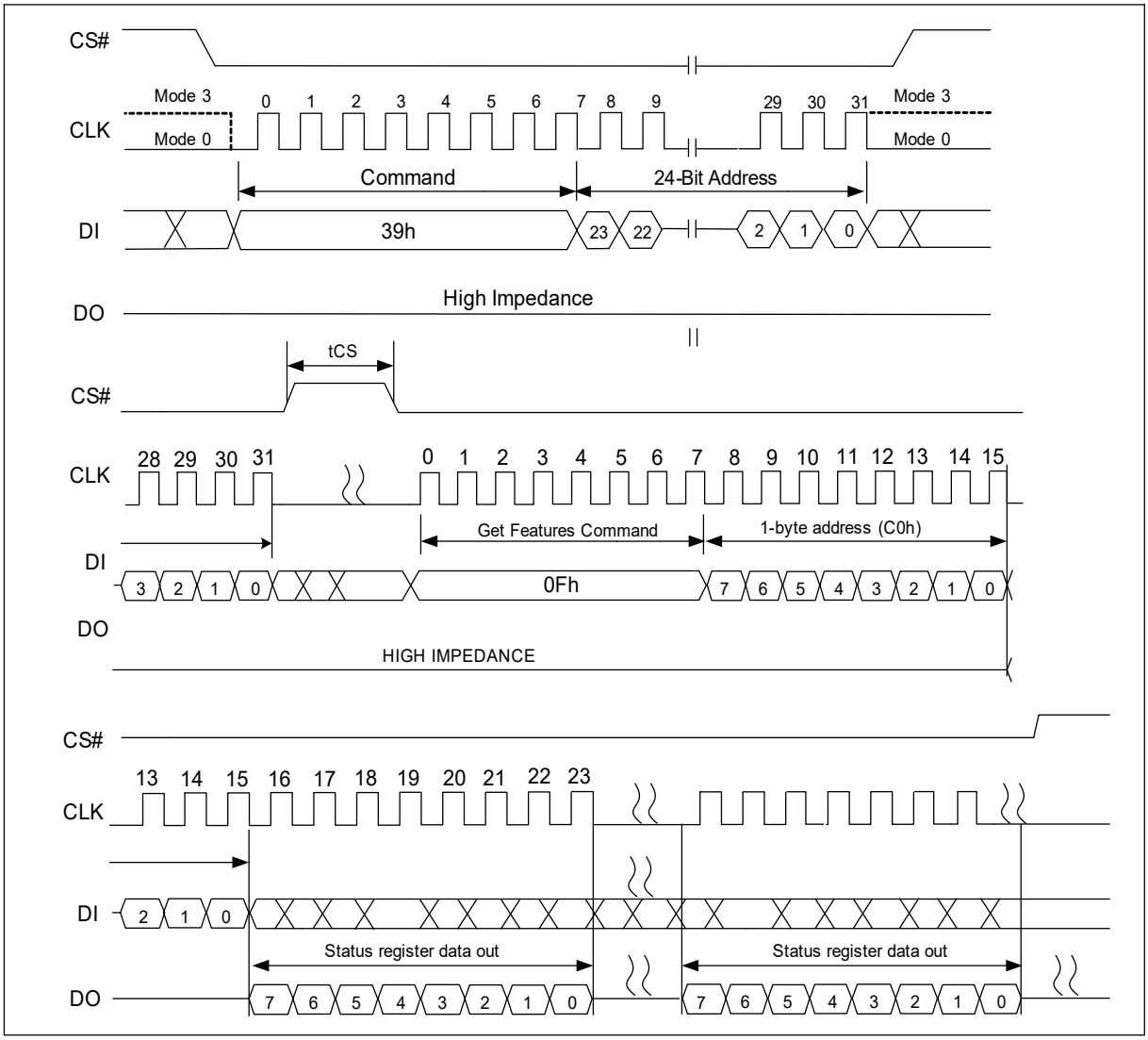
Figure 27 INDIVIDUAL BLOCK LOCK Command (36h) Timing



8.8.2. INDIVIDUAL BLOCK UNLOCK (39h)

The INDIVIDUAL BLOCK UNLOCK command requires a 24-bit address consisting of 2-bit '0' followed by a 10-bit block address (RA<5:0> is don't care) and 12 dummy bits. After the addresses are registered, the device starts clearing the corresponding INDIVIDUAL BLOCK LOCK bit, and is busy for t_{LCK} time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation.

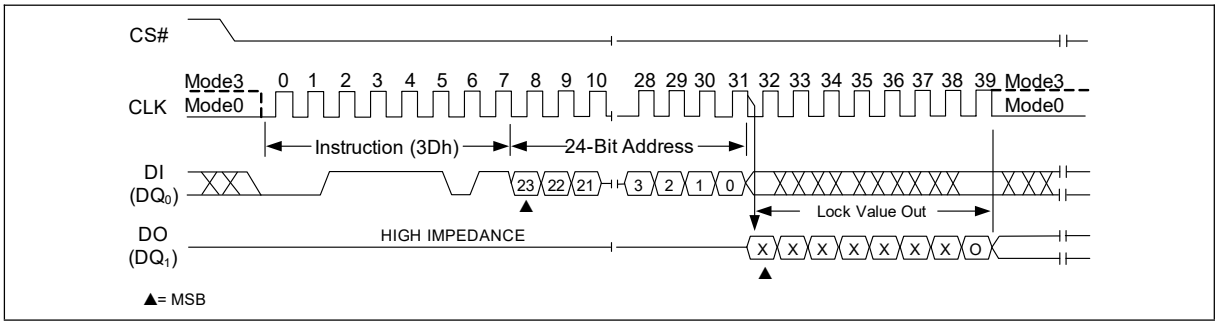
Figure 28 INDIVIDUAL BLOCK UNLOCK Command (39h) Timing



8.8.3. READ BLOCK LOCK (3Dh)

The READ BLOCK LOCK command can be used to read out the lock bit of a specific block. The READ BLOCK LOCK command requires a 24-bit address consisting of 2-bit '0' followed by a 10-bit block address (RA<5:0> is don't care) and 12 dummy bits. The Block Lock bit value will be shifted out on the DO pin at the falling edge of CLK shown in Figure 29. If the least significant bit (LSB) is 1, the corresponding block is locked; if LSB=0, the corresponding block is unlocked, ERASE/PROGRAM operation can be performed.

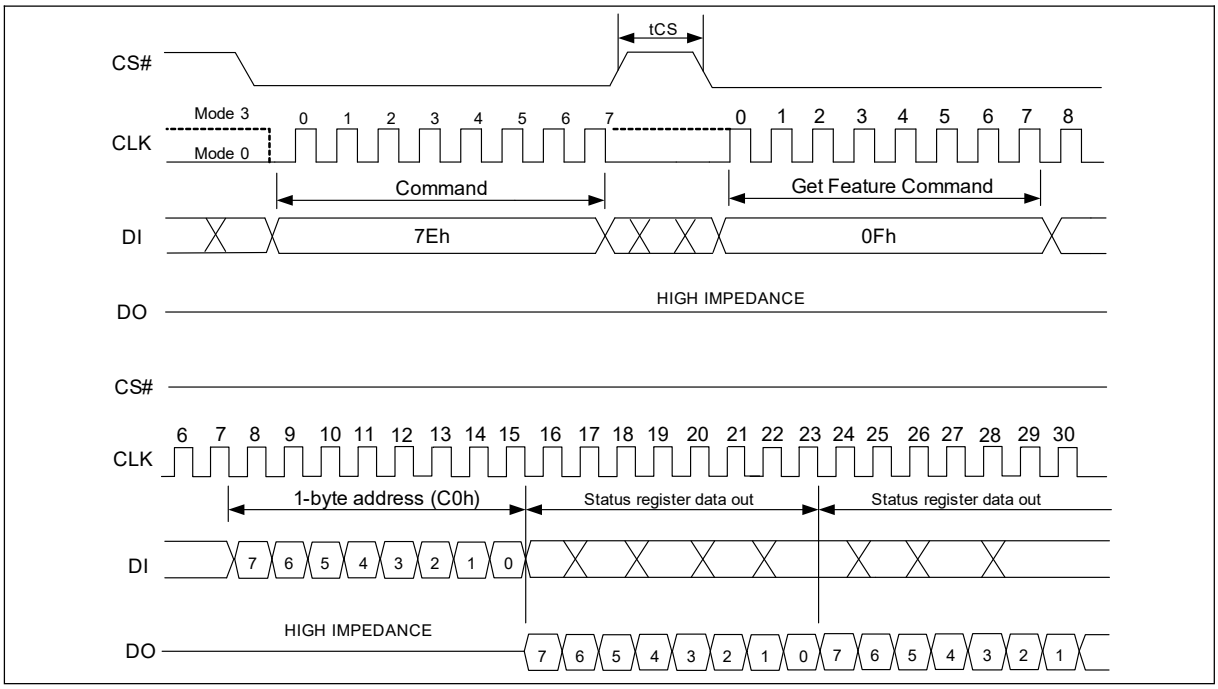
Figure 29 READ BLOCK LOCK Command (3Dh) Timing



8.8.4. GLOBAL BLOCK LOCK (7Eh)

All Block Lock bits can be set to 1 by the GLOBAL BLOCK LOCK instruction. After CS# being driven high as shown in Figure 30, the device starts setting all the INDIVIDUAL BLOCK LOCK bits, and is busy for t_{LCK} time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation.

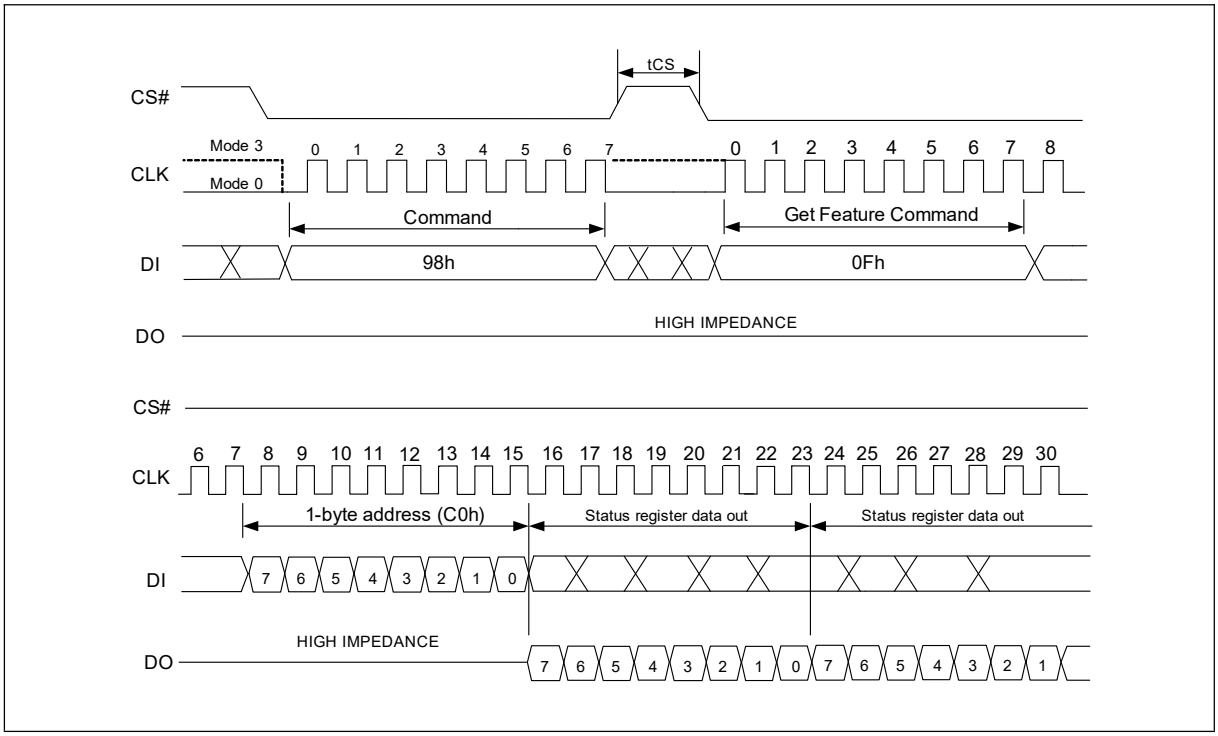
Figure 30 GLOBAL BLOCK LOCK Command (7Eh) Timing



8.8.5. GLOBAL BLOCK UNLOCK (98h)

All Block Lock bits can be cleared to 0 by the GLOBAL BLOCK UNLOCK instruction. After CS# being driven high as shown in Figure 31, the device starts clearing all the INDIVIDUAL BLOCK LOCK bits, and is busy for t_{LCK} time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation.

Figure 31 GLOBAL BLOCK UNLOCK Command (98h) Timing



9. Status Register

The device has an 8-bit status register that software can read during the device operation for operation state query. The status register can be read by issuing the GET FEATURES (0FH) command, followed by the feature address C0h (see Feature Operation).

Table 9 Status Register Bit Description

Bit	Bit Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared (P_FAIL = 0) during the PROGRAM EXECUTE command sequence or a RESET command.
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred (E_FAIL set to 1). It will also be set if the user attempts to erase an invalid address or a protected region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	WRITE ENABLE Latch	This bit indicates the current status of the WRITE ENABLE latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0) by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit is set when PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, RESET, GLOBAL BLOCK LOCK / UNLOCK or INDIVIDUAL BLOCK LOCK / UNLOCK is in progress, indicating the device is busy. During the busy state, do not input any command except 0Fh and FFh. When the bit is 0, the interface is in the ready state.
ECCS2 ECCS1 ECCS0	ECC Status	ECCS provides ECC Status as follows: 000b = No bit errors were detected during the previous read algorithm. 001b = Bit errors(<=3) were detected and corrected. 010b = Bit errors(=4) were detected and corrected. 011b = Bit errors(=5) were detected and corrected. 100b = Bit errors(=6) were detected and corrected. 101b = Bit errors(=7) were detected and corrected. 110b = Bit errors(=8) were detected and corrected. 111b = Internal error was detected and the data not promised correctly. Bit errors cannot be detected and corrected if their number exceeds the tolerance. Therefore, block data should be refreshed when ECC Status is equal to 110b. ECCS is set to 000b either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECCS is invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN).

10. OTP Region

The device offers a protected, One-Time Programmable NAND Flash memory area. Eight full pages (2176 bytes per page) are available on the device. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

To access the OTP feature, the user must issue the SET FEATURES command, followed by feature address B0h. When the OTP is ready for access, pages 00h–07h can be programmed in sequential order. The PROGRAM LOAD (02H) and PROGRAM EXECUTE (10H) commands can be used to program the pages (when not yet protected). Also, the PAGE READ (13H) command and READ FROM CACHE (03h/0Bh/3Bh/6Bh/BBh/EBh) commands can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in the table below.

Table 10 OTP States

OTP_PRT	OTP_EN	State
x	0	Normal Operation
0	1	Access OTP region
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10H) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data.

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

OTP Access

To access OTP, perform the following command sequence:

- Issue the SET FEATURES command (1Fh) to set OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

OTP Protect

- Issue the SET FEATURES command (1FH) to set OTP_EN and OTP_PRT
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command

11. Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory defect mapping requirements. See the following table for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Table 11 Error Management Details

Description	Requirement
Minimum number of valid blocks (N_{VB})	1003
Total available blocks per die	1024
First spare area location	Byte 2048
Bad-block mark	Non FFh

12. ECC Protection

The device offers data corruption protection by offering optional internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the “active” state.

To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1FH).
- Set the feature bit ECC_EN as you want:
  1. To enable ECC, Set ECC_EN to 1.
  2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

- The distribution of ECC segment is provided in the table below.
- ECC can protect according main and spare areas. When using the partial page program, the user area must be programmed simultaneously by the definition of ECC segment.
- Any data wrote to the ECC parity area are ignored.

Power on Read with internal ECC:
The device will automatically read first page of first block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correctly by internal ECC.

Table 12 ECC Segments

Min Byte Address	Max Byte Address	ECC Protected	Number Of Bytes	Area	Description
000H	1FFH	Yes	512	Main 0	User data 0
200H	3FFH	Yes	512	Main 1	User data 1
400H	5FFH	Yes	512	Main 2	User data 2
600H	7FFH	Yes	512	Main 3	User data 3
800H	80FH	Yes	16	Spare 0	User meta data 0(1)
810H	81FH	Yes	16	Spare 1	User meta data 1
820H	82FH	Yes	16	Spare 2	User meta data 2
830H	83FH	Yes	16	Spare 3	User meta data 3
840H	87FH	Yes	64	Spare Area	Internal ECC parity data

Note: 1. 800H is reserved for initial bad block mark, and please check the initial bad block mark with internal ECC off.

13. Electrical Characteristics

13.1. Absolute Maximum Ratings

Table 13 Absolute Maximum Ratings

Parameter	Value	Unit
Operating Temperature	-40 to +85	°C
Storage Temperature	-65 to +150	°C
Voltage on I/O Pin with Respect to Ground	-0.5 to 2.7	V
VCC	-0.5 to 2.7	V

Notes:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum input DC voltage on I/O pins is -0.5V. All I/O pins may have negative overshoot to VSS - 2.0V (range from VSS to VSS - 2.0V) during input voltage transitions from HIGH to LOW, for period up to 20ns (range from 0ns to 20ns), guaranteed by design and process. See Figure 32 for details.
3. Maximum input DC voltage on I/O pins is 2.7V. All I/O pins may have positive overshoot to VCC + 2.0V (range from VCC to VCC + 2.0V) during input voltage transitions from LOW to HIGH, for period up to 20ns (range from 0ns to 20ns), guaranteed by design and process. See Figure 33 for details.

Figure 32 Maximum Negative Overshoot Waveform

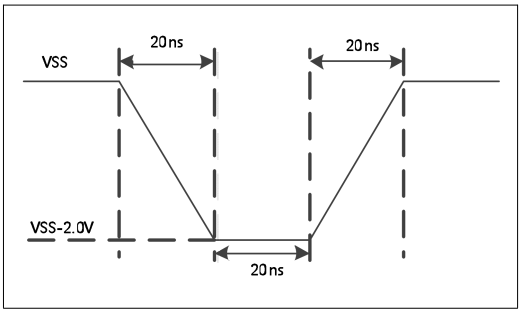
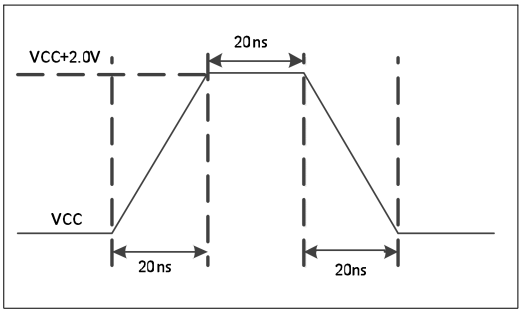


Figure 33 Maximum Positive Overshoot Waveform



13.2. Pin Capacitance

Table 14 Pin Capacitance

Applicable over recommended operating range from: T_A = +25°C.

Symbol	Test Condition	Max	Units	Conditions
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V
C_{OUT}(1)	Output Capacitance	8	pF	V_{OUT} = 0V

Notes:

1. Characterized and is not 100% tested.

13.3. Power-up and Power-Down Timing

Figure 34 Power-On Timing

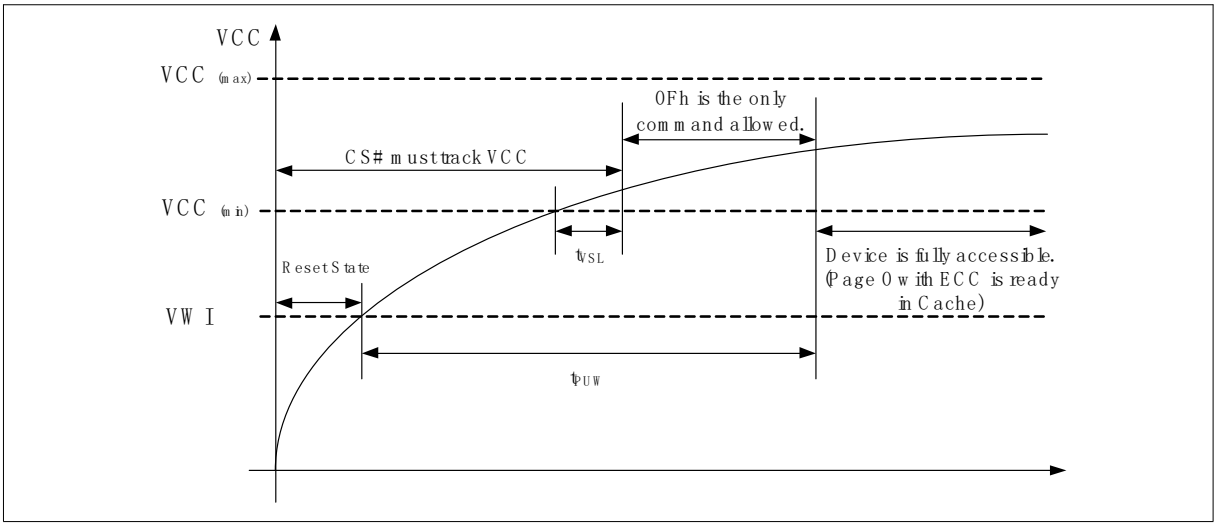


Table 15 Power-On Timing and Write Inhibit Threshold

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
t_{VSL}	VCC (min) to CS# Low	1		ms
t_{PUW}	Time Delay Before Write Instruction	12		ms
VWI	Write Inhibit Voltage		1.6	V

13.4. DC Electrical Characteristics

Table 16 DC Characteristics

Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 1.7V to 1.95V, (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
VCC	Supply Voltage		1.7		1.95	V
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	VCC=1.95V, CS# = VCC, V_{IN} = VSS or VCC		30	200	μA
I_{CC2}	Operating Current	CLK=0.1VCC/0.9VCC F_C=88MHz			40	mA
V_{IL}(1)	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}(1)	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100μA	VCC-0.2			V

Notes:

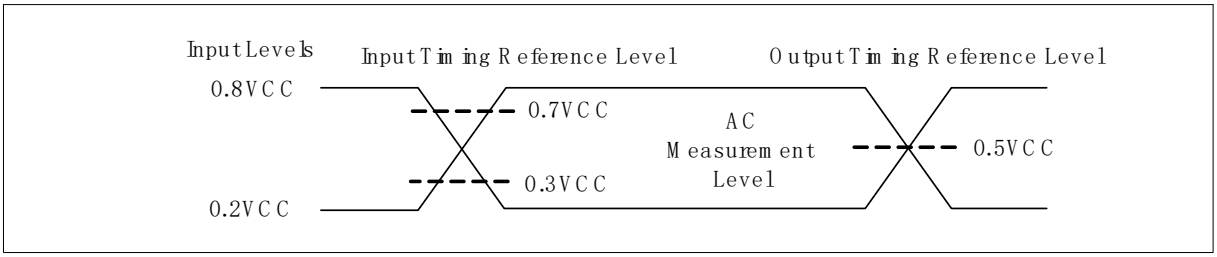
1. V_{ILmin} and V_{IHmax} are reference only and are not 100% tested.

13.5. AC Measurement Conditions

Table 17 AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN	MAX	
C_L	Load Capacitance		30	pF
T_R, T_F	Input Rise and Fall Times		5	ns
V_{IN}	Input Pulse Voltages	0.2VCC to 0.8VCC		V
IN	Input Timing Reference Voltages	0.3VCC to 0.7VCC		V
OUT	Output Timing Reference Voltages	0.5VCC		V

Figure 35 AC Measurement I/O Waveform



13.6. AC Electrical Characteristics

Table 18 AC Characteristics

Applicable over recommended operating range from: T_A= -40°C to +85°C, VCC= 1.7V to 1.95V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_C	Serial Clock Frequency for: all command			88	MHz
t_{CH1}	Serial Clock High Time	4.5			ns
t_{CL1}	Serial Clock Low Time	4.5			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}/t_{CS}	CS# High Time	20			ns
t_{SHQZ}	Output Disable Time			10	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}	HOLD# Low to High-Z Output			15	ns
t_{CLQV}	Output Valid from CLK			9	ns

SYMBOL	PARAMETER		SPEC			UNIT
			MIN	TYP	MAX	
t_{WHSL}	WP# Setup Time before CS# Low		20			ns
t_{SHWL}	WP# Hold Time after CS# High		100			ns
t_{LCK}	BLOCK LOCK/UNLOCK time	Individual			5	μs
		Global			32	
t_{IO_skew}	First IO to last IO data valid time				600	ps

Notes:

1. $t_{CH1} + t_{CL1} >= 1 / F_C$;
2. Value guaranteed by design and/or characterization, not 100% tested.

Table 19 Performance Timing

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
t_{RST}	CS# High to Next Command After Reset(FFh)			500	μs
t_{RD}	Page Read From Array (with ECC)		240	450	μs
	Page Read From Array (without ECC)		120	140	
t_{PROG}	Page Program (with ECC)			800	μs
	Page Program (without ECC)		400	700	
t_{ERS}	Block Erase		3	10	ms

Figure 36 Serial Output Timing

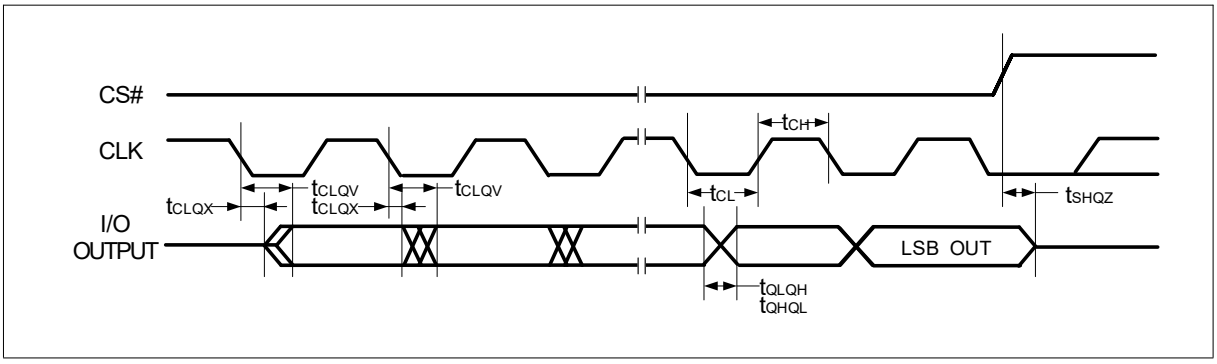


Figure 37 Serial Input Timing

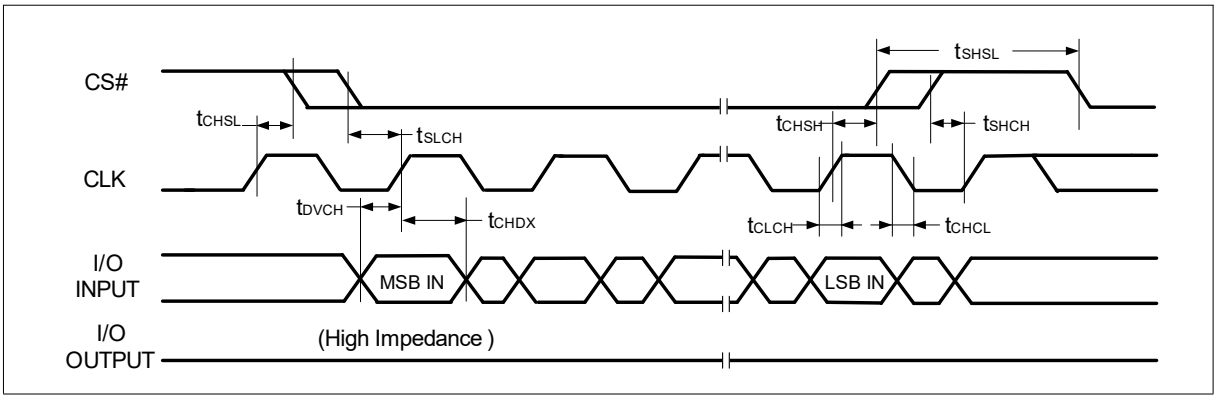


Figure 38 Hold Timing

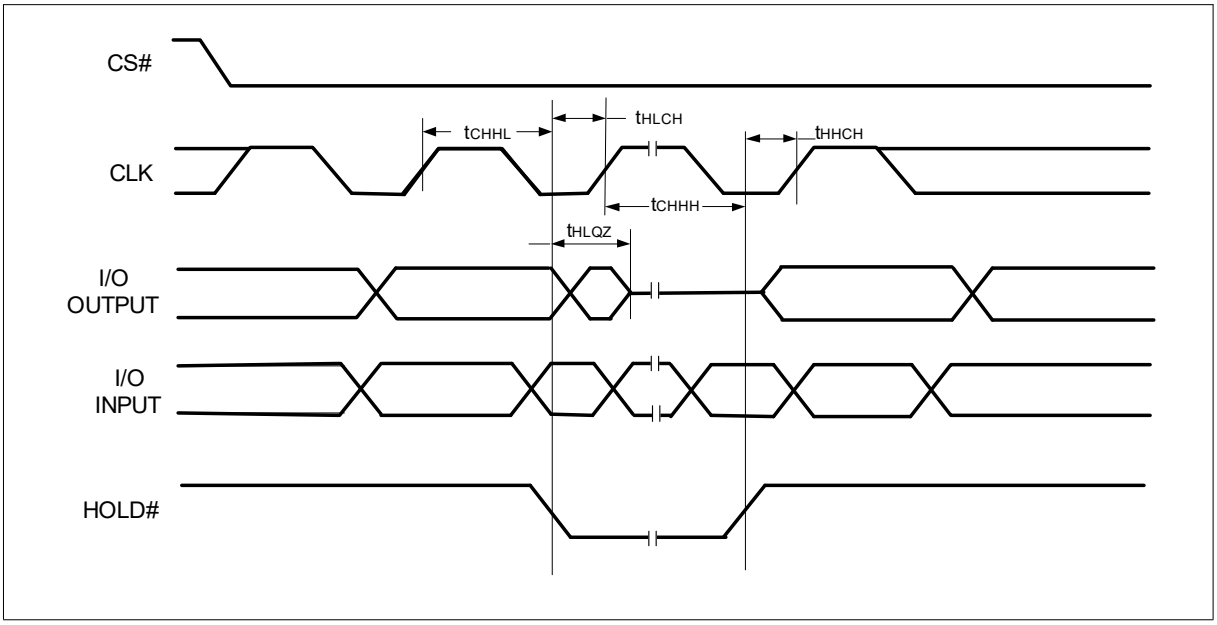
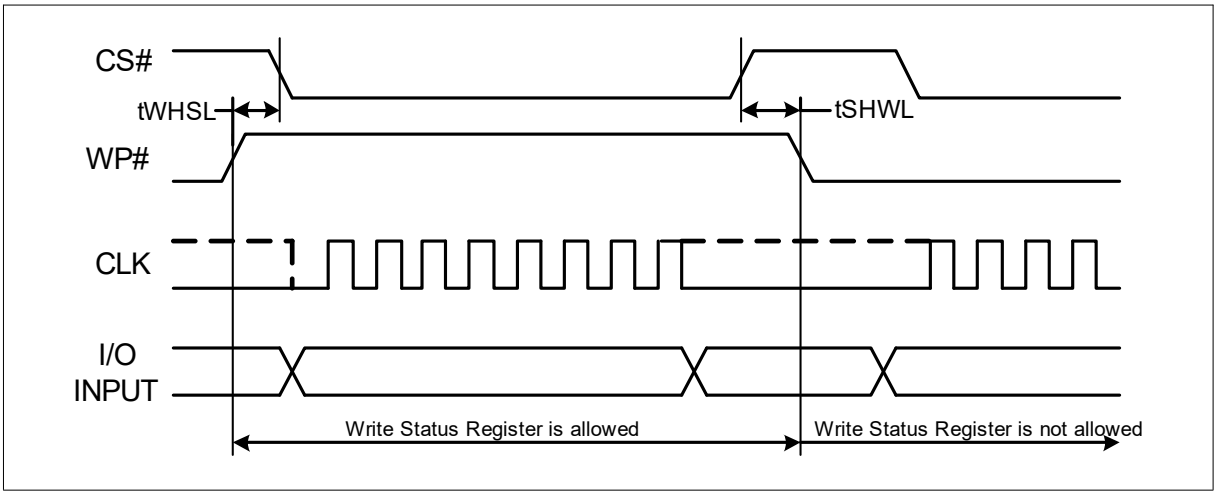


Figure 39 WP Timing



14. Ordering Information

FM 25LG 01 BI3 -XXX -C -H M

Company Prefix

FM = Fudan Microelectronics Group Co .,ltd

Product Family

25LG = 1.7~1.95V SPI NAND Flash

Product Density

01 = 1G-bit

Page Format Version

B = 2176-Byte / Page, ECC Protection Length 528-Byte / Phase
I3= Operating Range -40℃ ~+85℃

Package Type

DND = WSON8 8x6mm (TDFN8 8x6mm)

Product Carrier

A = Tray
T = Reel

HSF ID Code

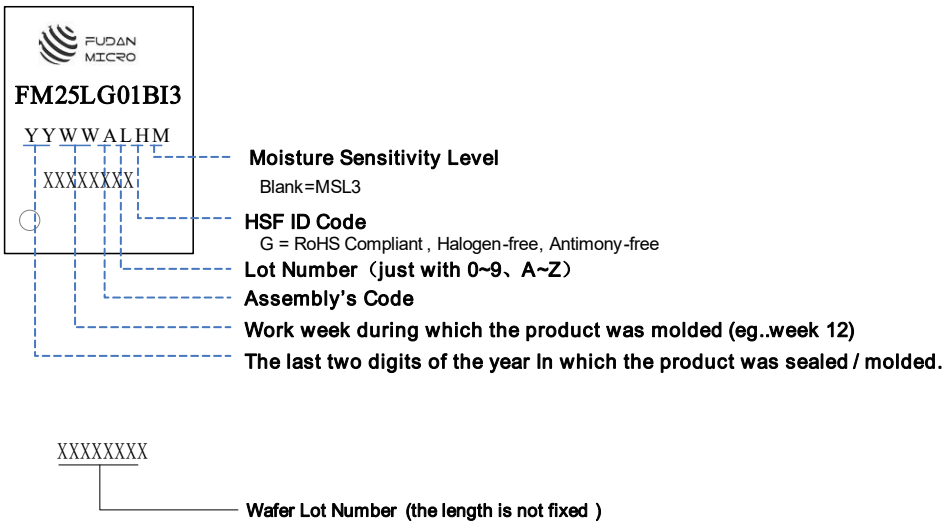
G = RoHS Compliant, Halogen-free, Antimony-free

MSL Level

3=MSL3

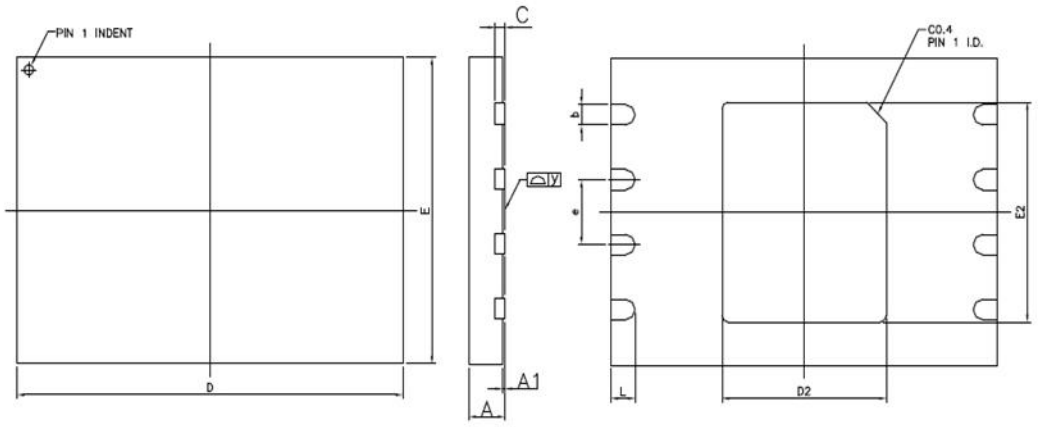
15. Part Marking Scheme

WSON8 8x6mm (TDFN8 8x6mm)



16. Packaging Information

WSON8 8x6mm (TDFN8 8x6mm)



Symbol	MIN	NOM	MAX
e		1.270 BSC	
D	7.900	8.000	8.100
E	5.900	6.000	6.100
L	0.400	0.500	0.600
A	0.700	0.750	0.800
A1	0.000	0.025	0.050
C		0.200 REF	
b	0.350	0.400	0.450
D2	3.300	3.400	3.500
E2	4.200	4.300	4.400

Note:
1. Dimensions are in Millimeters.

17. Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
preliminary	Apr. 2023	43		1. Initial Document Release
1.0	Sep. 2024	44		1. Updated the Packaging Information 2. Added Product Carrier Tape and Reel 3. Corrected typos

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