Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM25N256A
SPI Serial EEPROM

Data Sheet

Jan. 2024

Trademarks

1. Description

The FM25N256A provides 262,144 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 32,768 words of 8 bits each, with 128-bit UID and 64-byte Security Sector, and much improved the reliability by an internal ECC logic. The device is accessed through the SPI bus, and is optimized for automotive and industrial applications that require high reliability.

2. Features

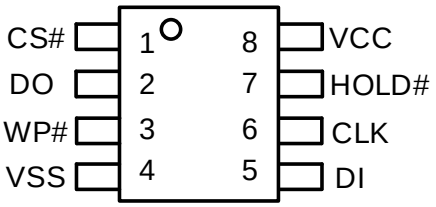
- **Low Operation Voltage: V_{CC} = 1.7V to 5.5V**
- **Serial Peripheral Interface (SPI) compatible**
- **Supports SPI Modes 0(0,0) and 3(1,1)**
- **20MHz clock rate(4.5V~5.5V) and 5MHz (1.7V)**
- **64-byte Page Mode and Byte Write operation supported**
- **Block write protection**
  - **Protect 1/4, 1/2, or entire array**
- **Write Protect (WP#) pin and Write Disable instructions for Hardware and software Data Protection**
- **Lockable 64-Byte Security Sector**
- **128-Bit Unique ID for each device**
- **Self-timed Write Cycle (5 ms max)**
- **Operating Temperature range:**
  - **-40°C to +85°C**
- **High-reliability**
  - **Endurance: 4 Million Write Cycles**
  - **Data Retention:100 Years**
  - **Built-in ECC Logic for Increased reliability**
  - **Enhance ESD Protection:⩾4KV**
  - **Prevention of Write Mistake at Low Voltage**
- **SOP8, TSSOP8 and TDFN8 Packages (RoHS Compliant and Halogen-free)**

3. Pin Configurations

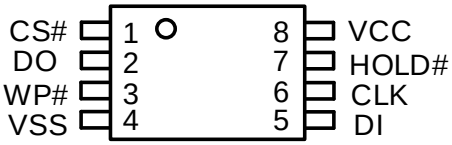
PIN NO.	PIN NAME	I/O	FUNCTION
1	CS#	I	Chip Select Input
2	DO	O	Data Output
3	WP#	I	Write Protect Input
4	VSS		Ground
5	DI	I	Data Input
6	CLK	I	Serial Clock Input
7	HOLD#	I	Hold Input
8	VCC		Power Supply

4. Packaging Type

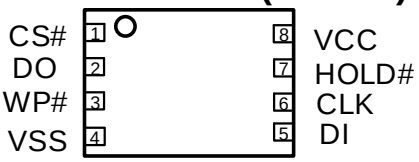
SOP 8



TSSOP8



TDFN8 (2x3mm)



5. Absolute Maximum Ratings

Ambient Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. Block Diagram

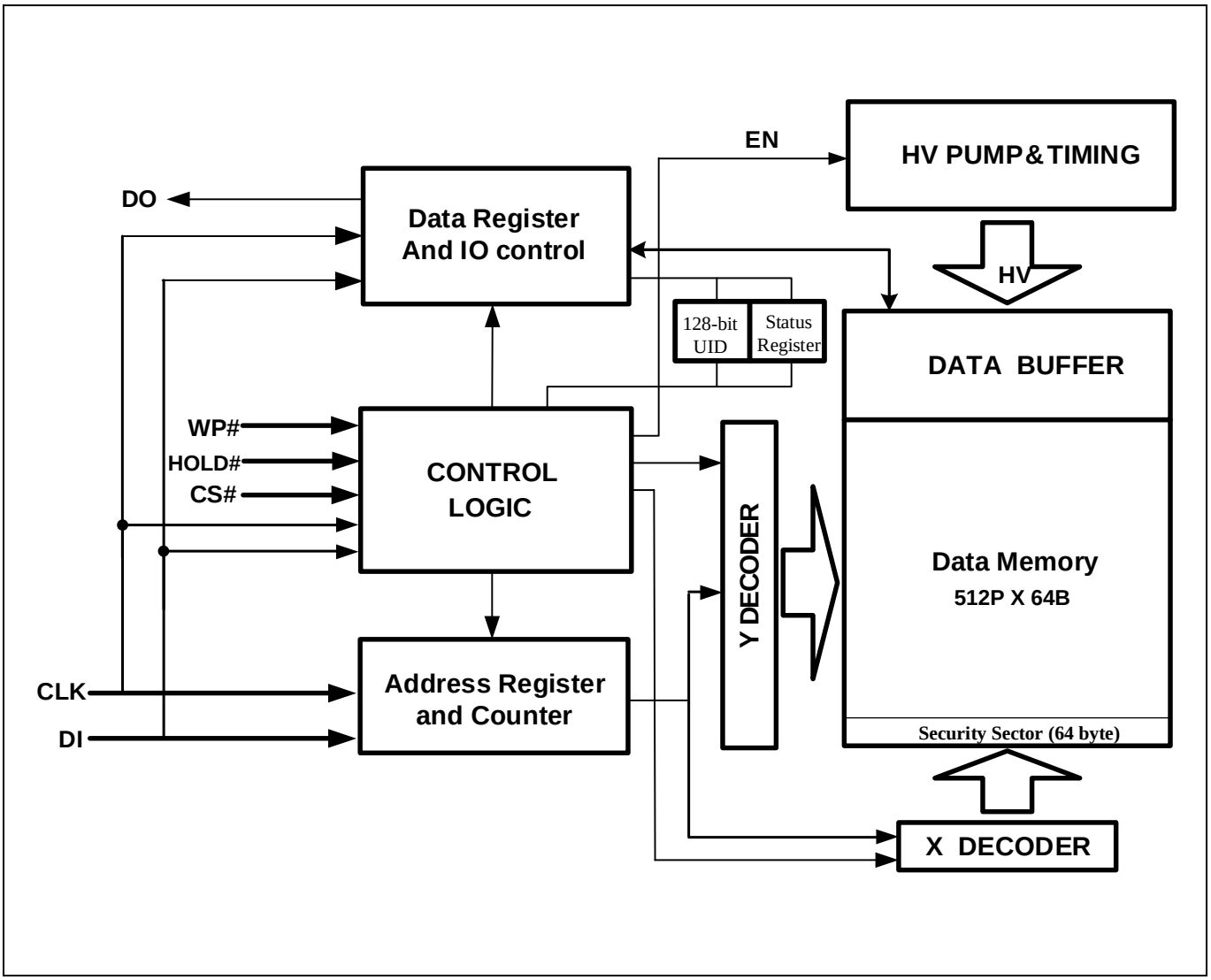


Figure 1 Block Diagram

7. Pin Descriptions

Serial Clock (CLK): The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

Serial Data Input (DI): The SPI Serial data input (DI) is used to serially receive write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin.

Serial Data Output (DO): The SPI Serial data output (DO) is used to read data or status from the device on the falling edge of CLK.

Chip Select (CS#): The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal write cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

HOLD (HOLD#): The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD# is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low.

Write Protect (WP#): The Write Protect (WP#) pin is used in conjunction with the Status Register Write Disable (SRWD) Bit to prevent the Status Registers from being written. Write Protect (WP#) pin and Status Register Write Disable (SRWD) Bit enable the device to be put in the Hardware Protected mode (when Status Register Write Disable (SRWD) Bit is set to 1, and Write Protect (WP#) pin is driven low).

8. Initial Delivery State

The device is delivered with:

- The memory array set to all "FFh" (each byte = FFh).
- Status register: bit SRWD =0, BP1 =0 and BP0 =0.
- Security Sector: The Security Sector is in a non-locked state, and all bytes are "FFh".

9. Memory Organization

Table 1 Memory Organization

Instruction	Page ADDR	Byte Number		
		63	…	0
0xh	0	Data Memory (512P X 64B)		
	1			
	2			
	…			
	511			
8xh	xxxx x00x xxxx xxxx[1]	Security Sector (64 Bytes)		
83h	xxxx xx1x xxxx xxxx[2]	Unique ID（128 Bits）		

Note:

1. Address bits A10A9 must be 00, A5~A0 define byte address, other bits are don't care
2. Address bits A10A9 must be x1, A3~A0 define byte address, other bits are don't care

10. Device Operations

10.1. Standard SPI

The FM25N256A is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial EEPROM. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

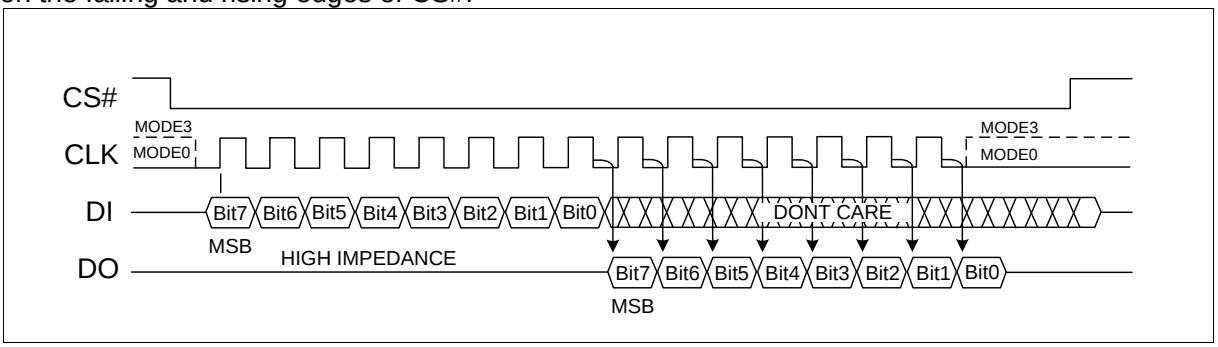


Figure 2 The difference between Mode 0 and Mode 3

10.2. Hold

For Standard SPI, the HOLD# signal allows the FM25N256A operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

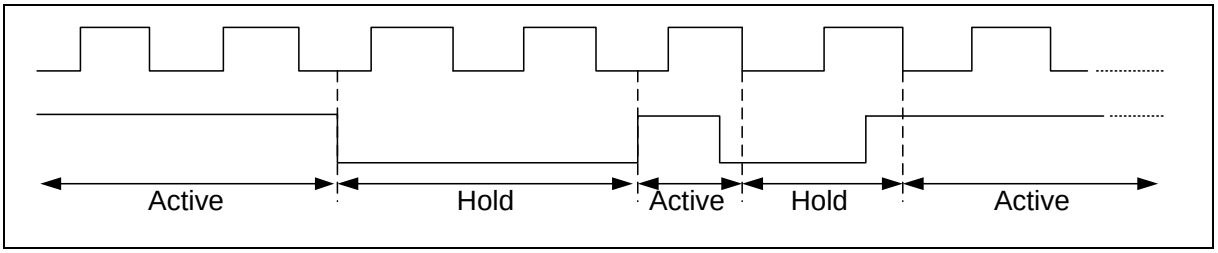


Figure 3 Hold Condition Waveform

11. Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the FM25N256A provides several means to protect the data from inadvertent writes.

Write Protect Features

- Write enable/disable instructions and automatic write disable after write
- Checking whether the number of clock pulses comprised in the instruction is a multiple of eight, before executing a write operation
- Software and Hardware (WP# pin) write protection using Status Register

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Write or Write Status Register instruction will be accepted. After completing a write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Block Protect (BP1 and BP0) bits. These settings allow top quarter (1/4), top half (1/2), or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information.

12. Status Register

The Read Status Register instruction can be used to provide status on the availability of the memory array, if the device is write enabled or disabled, the state of write protection. The Write Status Register instruction can be used to configure the device write protection features. Write access to the Status Register is controlled by the state of the non-volatile Status Register Write Disable bit (WRSD), the Write Enable instruction, and the WP# pin.

Factory default for all Status Register bits are 0.

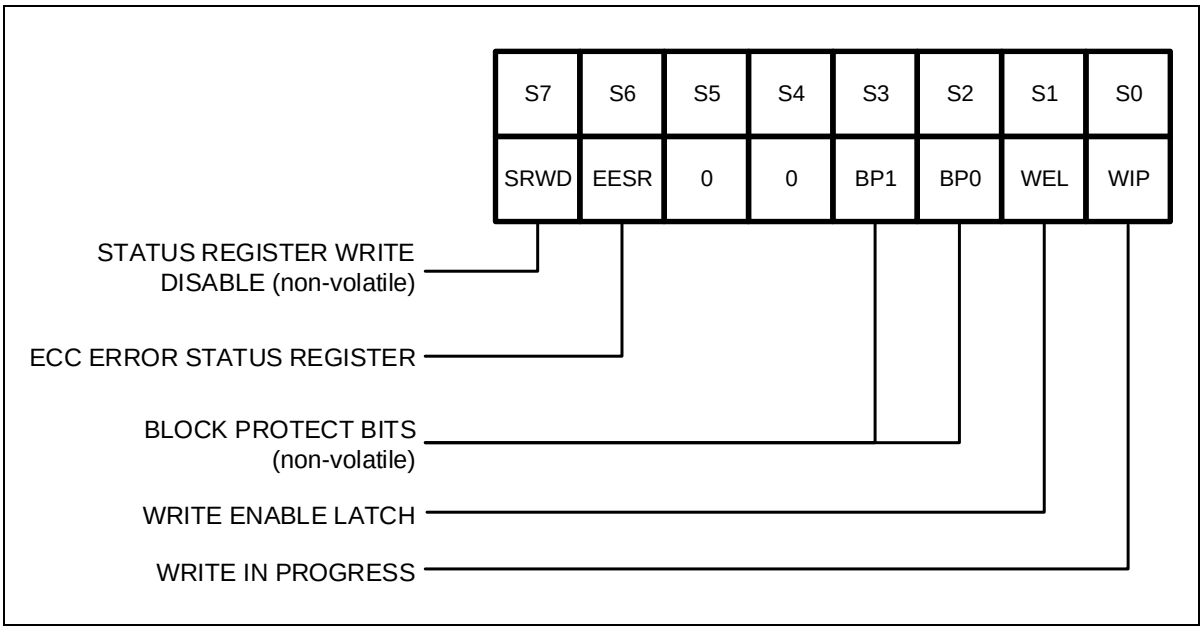


Figure 4 Status Register

12.1. WIP bit

WIP is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Write, Write Status Register instruction, Write Security Sector or Lock Security Sector. During this time the device will ignore further instructions except for the Read Status Register (see t_W in “14.3 AC Characteristics”). When the write, write status register, write Security Sector or lock Security Sector instruction has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

12.2. Write Enable Latch bit (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Write, Write Status Register, Write Security Sector, Lock Security Sector.

12.3. Block Protect bits (BP1, BP0)

The Block Protect Bits (BP1, BP0) are non-volatile read/write bits in the status register (S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in “14.3 AC Characteristics”). Top quarter (1/4), top half (1/2), or the entire memory array can be protected from write instructions (see Table 2 Status Register Memory Protection). The factory default setting for the Block Protection Bits is 0, none of the array protected.

12.4. ECC Error Status Register bit (EESR)

ECC Error Status Register (EESR) to indicate whether there is a single error bit in a group of four bytes during a Read operation. When EESR equals 1, it indicates that the ECC logic is performing an error correction operation during the current read operation. EESR equaling 0 signifies that the data read during the current read operation is correct and does not require any error correction.

If the users want to find the group address contains the error bit, according to the following steps:

- Start reading from the address of the user concerned. The Read operation must by group address, and then following the Read Status Register (RDSR) operation, and confirm the status of the EESR bit. If current group address is no error, then reading the next group address.
- Reading by group address and RDSR operation must be executed alternately until the error group address is found.
- The EESR bit will be set to logic ‘0b’ unless the previously executed read operation required the use of the ECC logic scheme. When this occurs, the EESR bit will set to logic ‘1’. The EESR bit will continue to read a logic ‘1’ until another read operation is issued and the use of the ECC logic scheme was not required or a Power-on Reset (POR) event occurred.

12.5. Status Register Write Disable bit (SRWD)

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Write Disable (SRWD) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

12.6. Status Register Memory Protection

Table 2 Status Register Memory Protection

level	Status Register Bits		Array Addresses Protected
	BP1	BP0	FM25N256A
0	0	0	None
1(1/4)	0	1	6000H – 7FFFH
2(1/2)	1	0	4000H – 7FFFH
3(All)	1	1	0000H – 7FFFH

13. Instructions

The Standard SPI instruction set of the FM25N256A consists of 11 basic instructions that are fully controlled through the SPI bus (see Table 3 Standard SPI Instructions Set). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in Figure 5 through Figure 15. All read instructions can be completed after any clocked bit. However, all instructions that Write must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the instruction will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being written, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the write cycle has completed.

13.1. Standard SPI Instructions Set

Table 3 Standard SPI Instructions Set

Instruction Name	Instruction Format	Operation
WREN	0000 0110	Set Write Enable Latch
WRDI	0000 0100	Reset Write Enable Latch
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory Array
WRITE	0000 0010	Write Data to Memory Array
Read Security Sector	1000 0011(1)	Read Security Sector
Write Security Sector	1000 0010(1)	Write Security Sector
Lock Security Sector	1000 0010(2)	Lock the Security Sector in Read-Only mode
Read Lock Status	1000 0011(2)	Read the lock status of the Security Sector
Read UID Number	1000 0011(3)	Read Unique ID Number

Note:
1. Address bits A10A9 must be 00, A5~A0 define byte address, all other bits are don't care
2. Address bits A10A9 must be 10, all other bits are don't care
3. Address bits A9 must be 1, A3~A0 define byte address, all other bits are don't care

13.2. Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Write and Write Status Register instruction. The Write Enable **(**WREN**)** instruction is entered by driving CS# low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

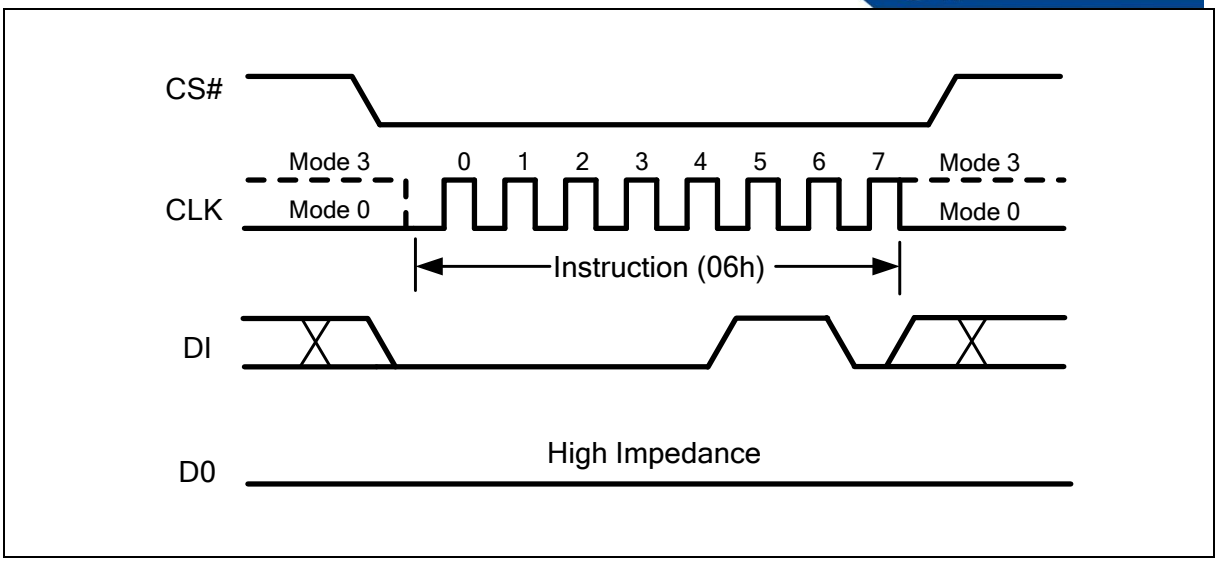


Figure 5 Write Enable Instruction

13.3. Write Disable (WRDI) (04h)

The Write Disable (WRDI) instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable (WRDI) instruction is entered by driving CS# low, shifting the instruction code “04h” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Write instructions.

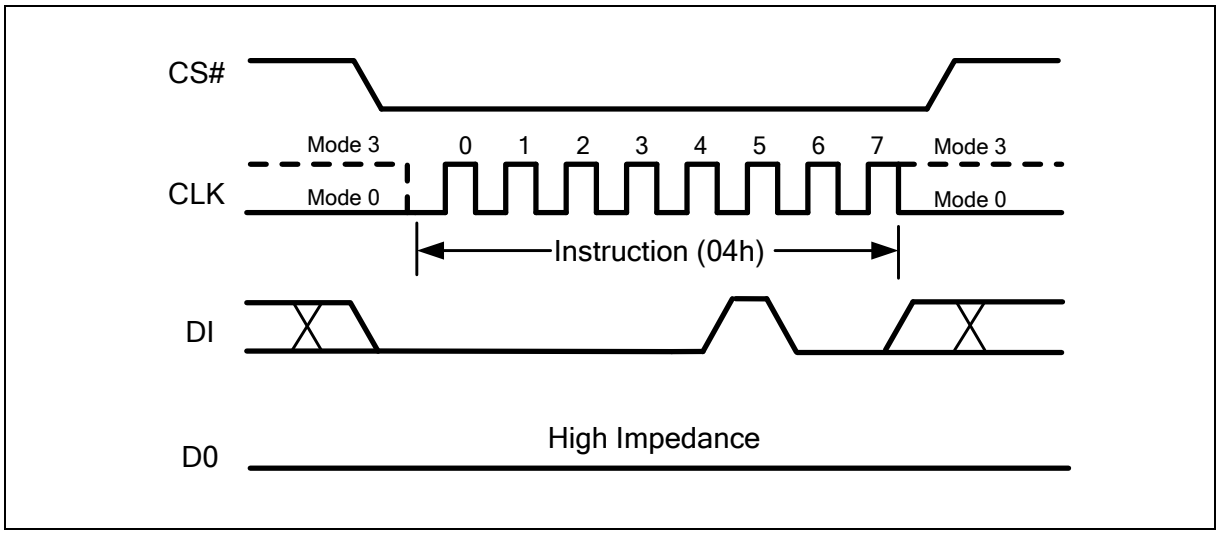


Figure 6 Write Disable Instruction

13.4. Read Status Register (RDSR) (05h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving CS# low and shifting the instruction code “05h” into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 7. The Status Register bits are shown in Figure 4 and include the WIP, WEL, BP1-BP0 and SRWD bits.

The Read Status Register instruction may be used at any time, even while a Write or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously. The instruction is completed by driving CS# high.

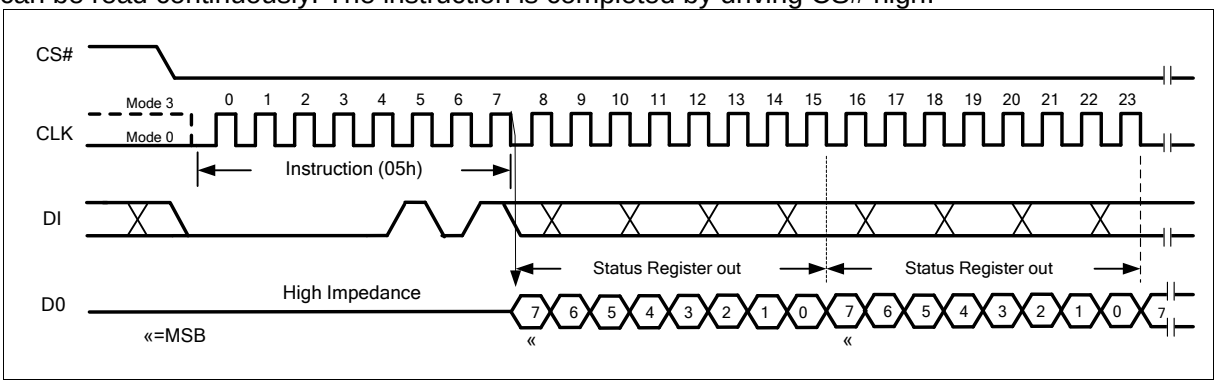


Figure 7 Read Status Register Instruction

13.5. Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows the Status Register to be written. Only non-volatile Status Register bits SRWD, BP1, BP0 can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register (WRSR) instruction. The Status Register bits are shown in Figure 4, and described in 12 Status Register.

To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register (WRSR) instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in Figure 8.

To complete the Write Status Register (WRSR) instruction, the CS# pin must be driven high after the eighth bit of data that is clocked in. If this is not done the Write Status Register (WRSR) instruction will not be executed.

During non-volatile Status Register write operation (06h combined with 01h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See “14.3 AC Characteristics”). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

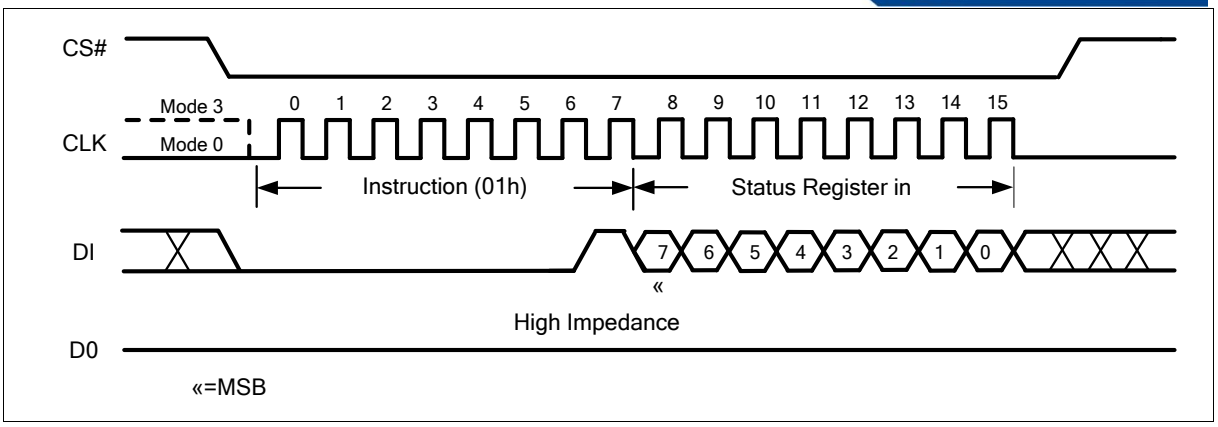


Figure 8 Write Status Register Instruction

13.6. Read from Memory Array (03h)

The Read instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 16-bit address A15-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read instruction sequence is shown in Figure 9. If a Read Data instruction is issued while an Write cycle is in process (WIP =1) the instruction is ignored and will not have any effect on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_c (see “14.3 AC Characteristics”).

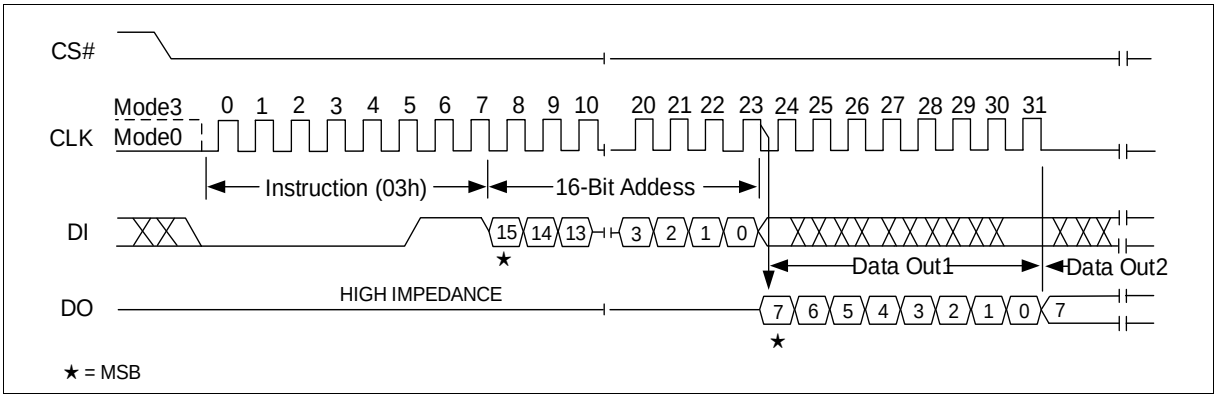


Figure 9 Read Data Instruction

13.7. Write to Memory Array (02h)

The Write instruction allows from one byte to 64 bytes (a page) of data to be written. A Write Enable instruction must be executed before the device will accept the Write Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 16-bit address A15-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Write instruction sequence is shown in Figure 10.

If an entire 64 byte page is to be programmed, the last address byte (the 6 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 64 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 64 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write instruction will not be executed. After CS# is driven high, the self-timed Write instruction will commence for a time duration of t_w (See "14.3 AC Characteristics"). While the Write cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Write cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Write cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Write instruction will not be executed if the addressed page is protected by the Block Protect (BP1 and BP0) bits.

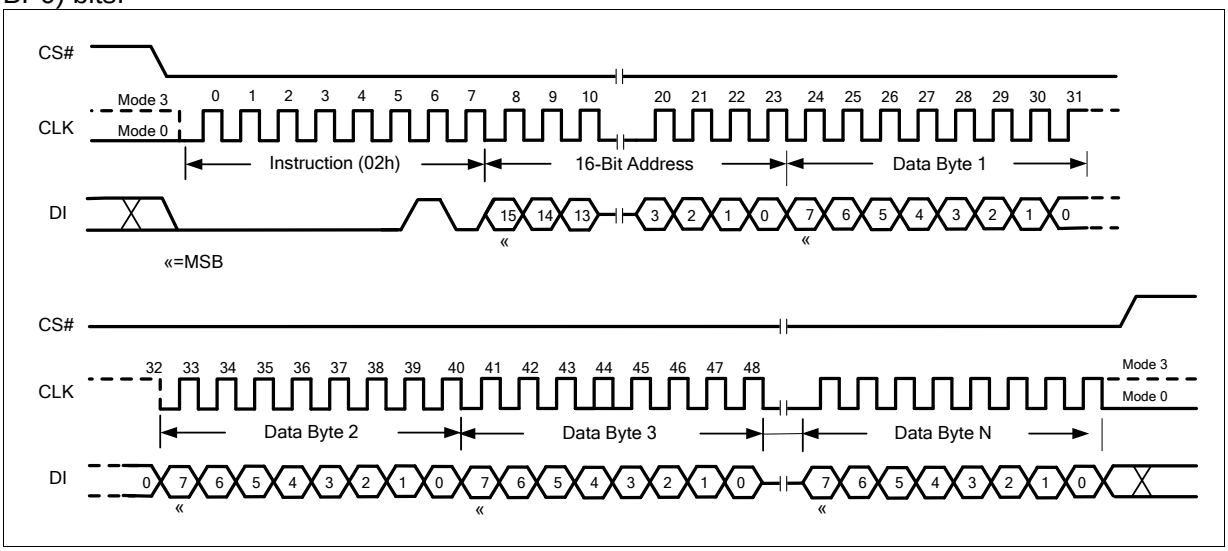


Figure 10 Page Program Instruction

13.8. Read Security Sector (83h)

The FM25N256A offers 64-byte Security Sector which can be written and (later) permanently locked in Read-only mode.

The Read Security Sector instruction is similar to the Read instruction and allows one or more data bytes to be sequentially read from Security Sector. The instruction is initiated by driving the initiated by driving the CS# pin low and then shifting the instruction code "83h" followed by a 16-bit address A15-A0 into the DI pin. Address bits A10A9 must be 00, upper address bits are don't care. The data byte pointed to by the lower address bits [A5:A0] is shifted out on DO pin. If Chip Select (CS#) continues to be driven low, the byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte 7Fh), it will be reset to 00h, the first byte of the register, and continue to increment. The instruction is completed by driving CS# high. The Read Security Sector instruction sequence is shown in Figure 11.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

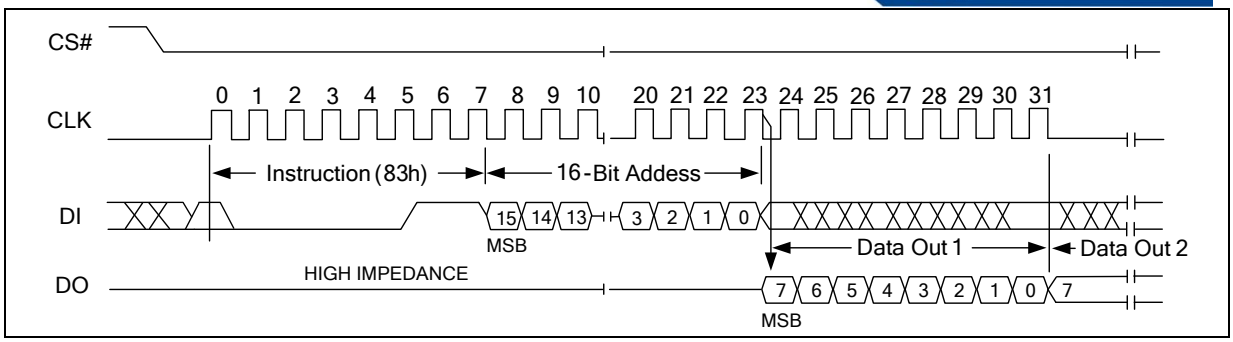


Figure 11 Read Security Sector Sequence

13.9. Write Security Sector (82h)

The Write Security Sector instruction is similar to the Write instruction. It allows from one byte to 64 bytes of Security Sector data to be written. A Write Enable instruction must be executed before the device will accept the Write Security Sector Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “82h” followed by a 16-bit address A15-A0 and at least one data byte, into the DI pin. Address bit A10A9 must be 00, upper address bits are don’t care, the lower address bits [A5:A0] address bits define the byte address inside the Security Sector. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device.

The instruction is discarded, and is not executed if the Block Protect bits (BP1,BP0) = (1,1) or the Security Sector has been locked.

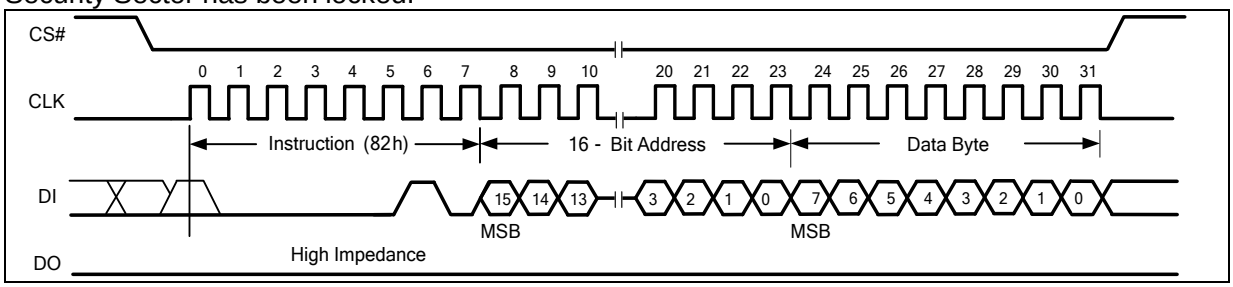


Figure 12 Write Security Sector Sequence

13.10. Lock Security Sector (82h)

The Lock Security Sector instruction permanently locks the Security Sector in Read-only mode. Before this instruction can be accepted, a Write Enable instruction must have been executed. The Lock Security Sector instruction is initiated by driving the CS# pin low, then shifting the instruction code “82h” followed by a 16-bit address A15-A0 and one data byte, into the DI pin. Address bits A10A9 must be 10, all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care.

The CS# pin must be driven high after the rising edge of CLK that latches in the eighth bit of the data byte, and before the next rising edge of CLK. Otherwise, the Lock Security Sector instruction is not executed.

The instruction is discarded, and is not executed if the Block Protect bits (BP1,BP0) = (1,1) or the Security Sector has been locked.

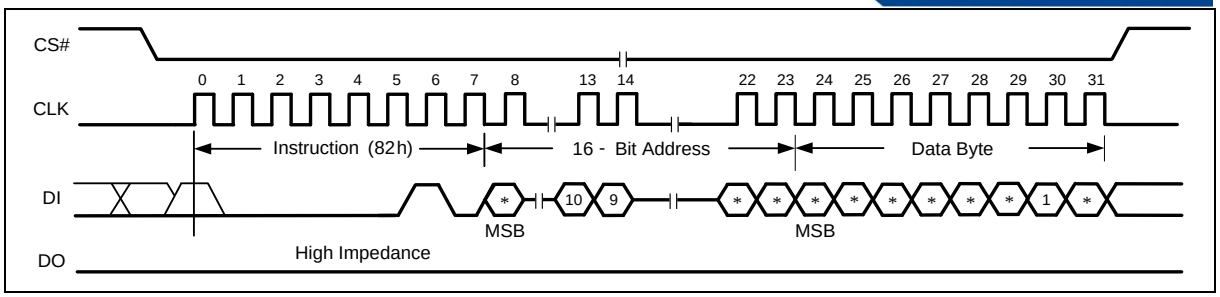


Figure 13 Lock Security Sector Sequence

13.11. Read Lock Status (83h)

The Read Lock Status instruction is used to check whether the Security Sector is locked or not in Read-only mode. The Read Lock Status instruction is initiated by driving the CS# pin low, then shifting the instruction code “83h” followed by a 16-bit address A15-A0 into the DI pin. Address bits A10A9 must be 10, all other address bits are Don't Care. The Lock bit is the BIT1 of the byte read on DO pin. It is at “1” when the lock is active and at “0” when the lock is not active. If CS# pin continues to be driven low, the same data byte is shifted out. The read cycle is terminated by driving CS# pin high.

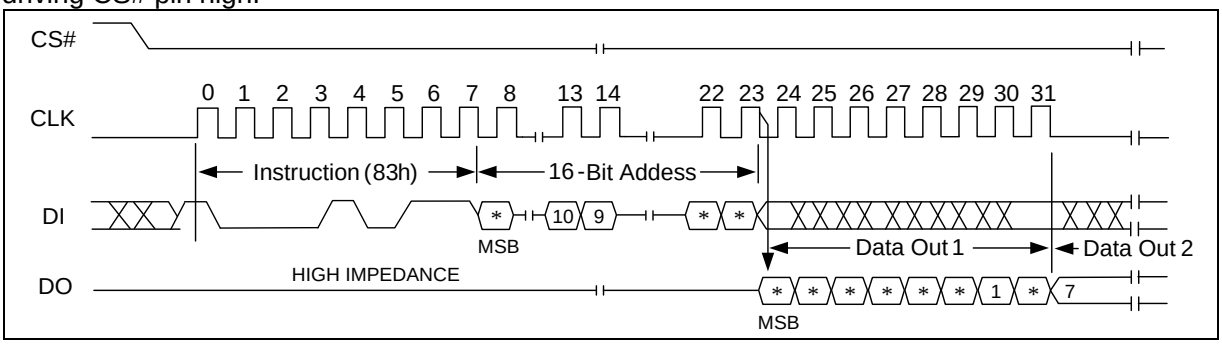


Figure 14 Read Lock Status Sequence

13.12. Read UID Number (83h)

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each FM25N256A device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code “83h” followed by a 16-bit address A15-A0 into the DI pin. Address bit A9 must be ‘1b’, upper address bits are don’t care, the lower address bits [A3:A0] define the byte address inside the UID. After which, the 128-bit ID is shifted out on the falling edge of CLK as shown in Figure 15. When the end of the 128-bit UID number is reached (16 bytes of data), the data word address will roll-over back to the beginning of the 128-bit UID number. The read UID cycle is terminated by driving CS# pin high.

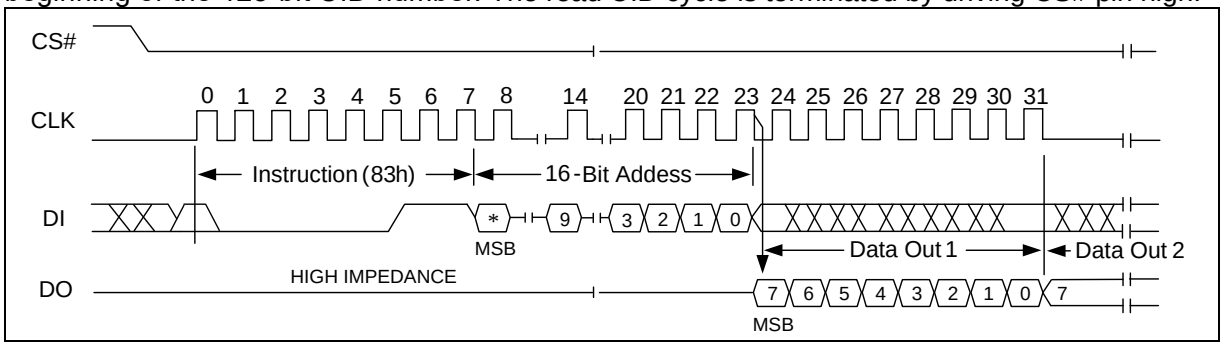


Figure 15 Read UID Number Sequence

14. Electrical Characteristics

14.1. DC Electrical Characteristics

Table 4 DC Electrical Characteristics

Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Max	Units
V_{CC}	Supply Voltage		1.7	5.5	V
I_{CC1}	Supply Current (Read)	V_{CC} = 1.7V at 5 MHz DO = Open, CLK=0.1Vcc/0.9Vcc		1.0	mA
		V_{CC} = 2.5V at 10 MHz DO = Open, CLK=0.1Vcc/0.9Vcc		2.0	mA
		V_{CC} = 5.5V at 20 MHz DO = Open, CLK=0.1Vcc/0.9Vcc		5.0	mA
I_{CC2}	Supply Current (Write)	V_{CC} = 5.5V, during tw, CS# = Vcc		3.0	mA
		V_{CC} = 1.7V, during tw, CS# = Vcc		2.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V, CS# = V_{CC}, V_{IN} = V_{CC}/ V_{SS}		2.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V, CS# = V_{CC}, V_{IN} = V_{CC}/ V_{SS}		3.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.5V, CS# = V_{CC}, V_{IN} = V_{CC}/ V_{SS}		6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}/V_{SS}	-2.0	2.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}/ V_{SS}	-2.0	2.0	µA
V_{IL}[1]	Input Low Level	1.7V ≤ VCC < 2.5V	-0.45	V_{CC} x 0.2	V
		2.5V ≤ VCC < 5.5V	-0.45	V_{CC} x 0.3	V
V_{IH}[1]	Input High Level	1.7V ≤ VCC < 2.5V	V_{CC} x 0.8	V_{CC} + 0.5	V
		2.5V ≤ VCC < 5.5V	V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Level 1	V_{CC} = 3.6V, I_{OL} = 3.0 mA		0.4	V
V_{OH1}	Output High Level 1	V_{CC} = 3.6V, I_{OH} = -1.6 mA	V_{CC} -0.8		
V_{OL2}	Output Low Level 2	V_{CC} =1.7V, I_{OL} = 0.15 mA		0.2	V
V_{OH2}	Output High Level 2	V_{CC} =1.7V, I_{OH} = -100 uA	V_{CC} -0.2		

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

14.2. AC Measurement Conditions

Table 5 AC Measurement Conditions

SYMBOL	PARAMETER	SPEC		UNIT
		MIN.	MAX.	
CL	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		25	ns
VIN	Input Pulse Voltages	0.2 V_{CC} to 0.8 V_{CC}		V
IN	Input Timing Reference Voltages	0.3 V_{CC} to 0.7 V_{CC}		V
OUT	Output Timing Reference Voltages	0.5V_{CC}		V

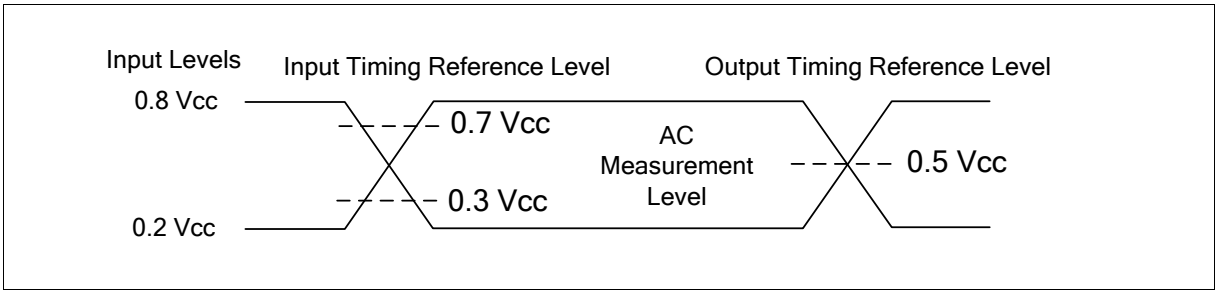


Figure 16 AC Measurement I/O Waveform

14.3. AC Characteristics

Table 6 AC Characteristics

Recommended operating conditions: T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V.

SYMBOL	PARAMETER	V_{CC}≥1.7V		V_{CC}≥2.5V		V_{CC}≥4.5V		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_C	Clock frequency		5		10		20	MHz
t_{SLCH}	CS# active setup time	60		30		15		ns
t_{SHCH}	CS# not active setup time	60		30		15		ns
t_{SHSL}	CS# deselect time	90		40		20		ns
t_{CHSH}	CS# active hold time	60		30		15		ns
t_{CHSL}	CS# not active hold time	60		30		15		ns
t_{CH} (1)	Clock high time	80		55		20		ns
t_{CL} (1)	Clock low time	80		40		20		ns
t_{CLCH} (2)	Clock rise time		2		2		2	us
t_{CHCL} (2)	Clock fall time		2		2		2	us
t_{DVCH}	Data in setup time	20		10		5		ns
t_{CHDX}	Data in hold time	20		10		10		ns
t_{HHCH}	Clock low hold time after HOLD# not active	60		30		15		ns
t_{HLCH}	Clock low hold time after HOLD# active	60		30		15		ns
t_{CLHL}	Clock low setup time before HOLD# active	0		0		0		ns
t_{CLHH}	Clock low setup time before HOLD# not active	0		0		0		ns
t_{SHQZ}	Output disable time		80		40		20	ns
t_{CLQV}	Clock low to output valid		80		40		20	ns

SYMBOL	PARAMETER	V_{CC}≥1.7V		V_{CC}≥2.5V		V_{CC}≥4.5V		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{CLQX}	Output hold time	0		0		0		ns
t_{QLQH}	Output rise time		20		20		10	ns
t_{QHQL}	Output fall time		20		20		10	ns
t_{HHQV}	HOLD# high to output valid		80		40		20	ns
t_{HLQZ}	HOLD# low to output High-Z		80		40		20	ns
t_W	Write time		5		5		5	ms

Notes:

1. $t_{CH}+t_{CL} >= 1/f_C$;
2. This parameter is characterized and is not 100% tested.

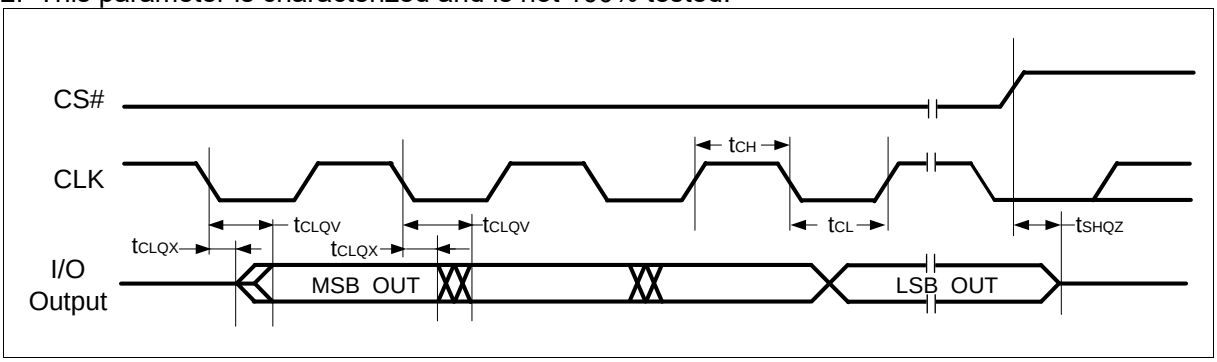


Figure 17 Serial Output Timing

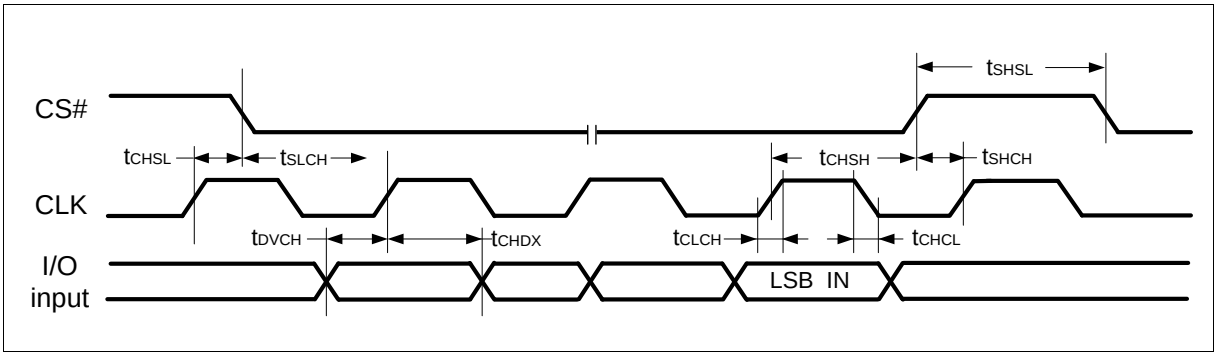


Figure 18 Serial Input Timing

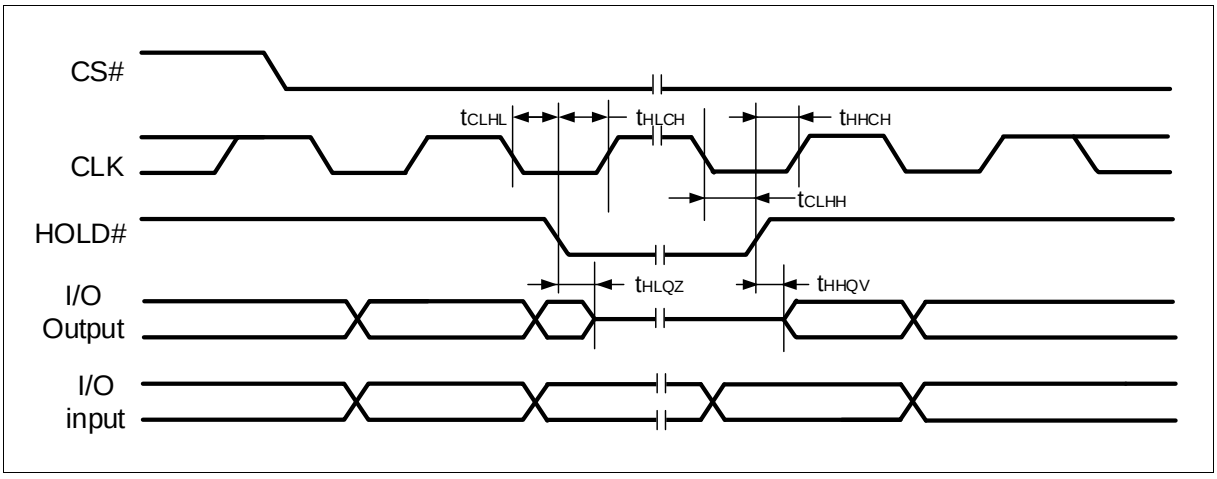


Figure 19 Hold Timing

14.4. Pin Capacitance

Table 7 Pin Capacitance

PARAMETER	SYMBOL	CONDITIONS	Max	Units
Input Capacitance	C_{IN}[1]	V_{IN} = 0V, f = 5 MHz	6	pF
Output Capacitance	C_{OUT}[1]	V_{OUT} = 0V, f = 5 MHz	8	pF

Note: 1. This parameter is characterized and is not 100% tested.

15. Cycling Performance

PARAMETER	SYMBOL	Test Condition	Max	Units
Write cycle endurance	Ncycle	T_A = 25 °C, Page Mode $V_{CC(min)}$ < V_{CC} < $V_{CC(max)}$,	4,000,000	Write cycle

Note:

1. This parameter is characterized and qualification. It is not 100% tested.
2. The Write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer.
3. A Write cycle is executed when either a Page Write, a Byte Write, a Write Security Sector or a Lock Security instruction is decoded. When using these instructions, refer also to Section: Cycling with Error Correction Code (ECC) on page 22.

16. Data Retention

PARAMETER	Test Condition	Min	Units
Data retention	T_A = 55 °C	100	Year

Note:
1. This parameter is characterized and qualification. It is not 100% tested.

17. Recommendations for Application Design

17.1. Power Supply (V_{CC})

A stable V_{CC} voltage within the range specified in [V_{CC}(min),V_{CC}(max)] must be applied prior to selecting the memory and issuing instructions. See Table 4.
This voltage should remain stable and valid throughout the instruction transmission and, in the case of a Write instruction, until the internal Write cycle (t_W) is completed. To ensure a stable DC supply, place a capacitor of suitable capacitance (normally between 10nF and 100nF) close to the V_{CC}/V_{SS} package pins to decouple the V_{CC} line.

17.2. Power-up Timing Requirements

To prevent write operations or other spurious events from occurring during power-up, the FM25N256A includes a power-on reset (POR) circuit.

The system designer must ensure that instructions are not sent to the device until the Vcc supply has reached a stable value, greater than or equal to the minimum Vcc level. Additionally, once the Vcc is greater than or equal to the minimum Vcc level, the host must wait at least t_{INIT} before sending the first command to the device. See Table 8 for the values associated with these power-up parameters.

If an event occurs in the system where the Vcc level supplied to the FM25N256A drops below the maximum V_{POR} level specified, it is recommended that a full-power cycle sequence be performed by first driving the Vcc pin to Vss, waiting at least the minimum t_{POFF} time and then perform a new power-up sequence in compliance with the requirements defined in Table 8.

During a power-up sequence, the Vcc supplied to the FM25N256A should monotonically rise from Vss to the minimum Vcc level, as specified in Table 8.

Figure 20. V_{CC} Ramp Up and Ramp Down

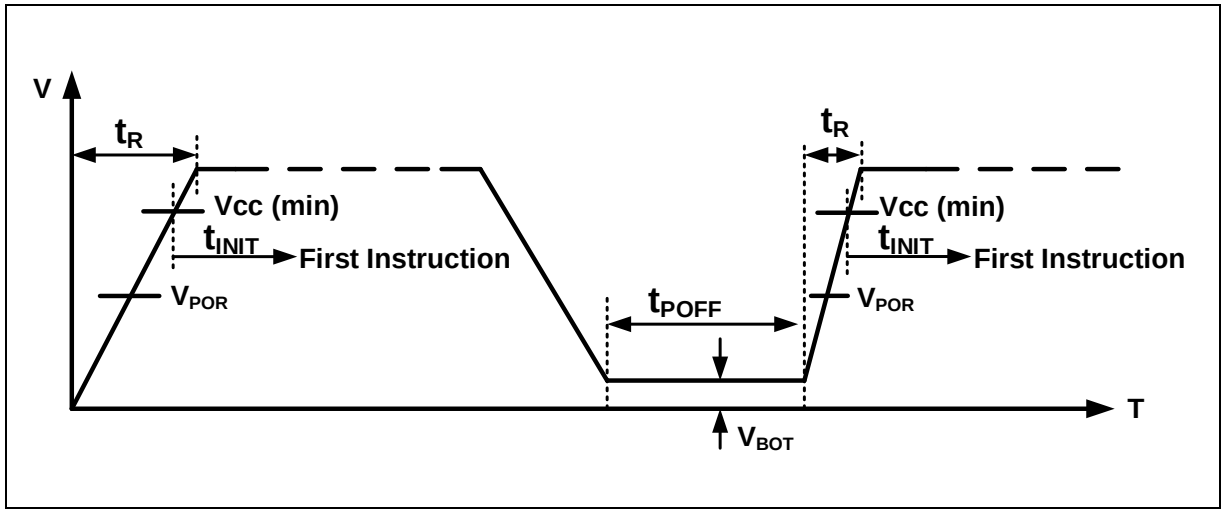


Table 8 Power-up Timing Characteristics

Symbol	Parameter	Test Condition	Min	Max	Units
t_R	Power on time		0.001	2000	ms
t_{POFF}	power cycle off time		300		us
t_{INIT}	Time from power on to first command		1		ms
V_{BOT}	Power Off threshold for the next power on cycle	No ringback above V_{Bot}		0.7	V
V_{POR}	Power-On Reset threshold voltage			1.3	V

Note: V_{CC} must rise monotonically without ringback.

17.3. Low Voltage Malfunction Prevention Function

The FM25N256A has a built-in detection circuit which prevents data rewrite operation at low power, and prevents write or read operation error. At V_{DET} or lower, rewriting of data is prevented (Refer to Figure 21).

Figure 21. Operation during Low Power Supply Voltage

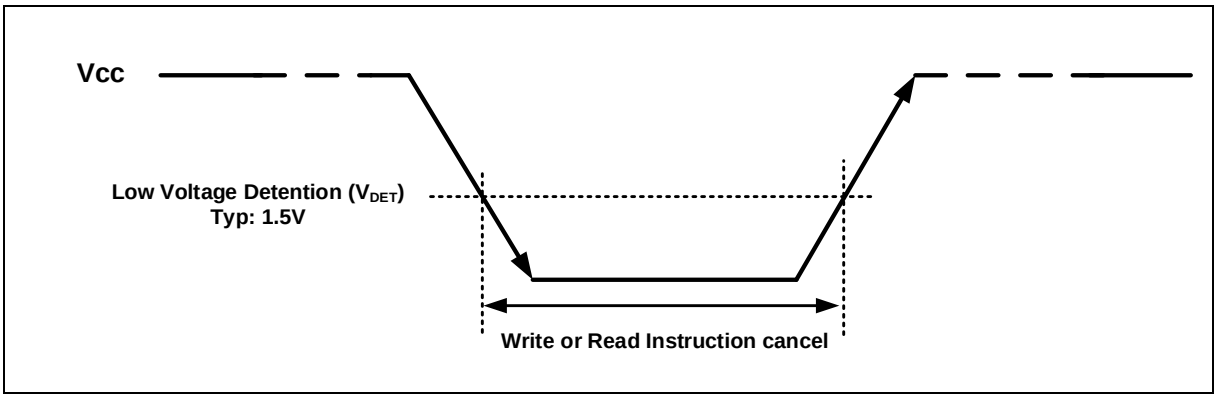


Table 9 V_{DET} parameters

Symbol	Parameter	Test Condition	Min	Max	Units
V_{DET}	Low power detention voltage			1.5	V

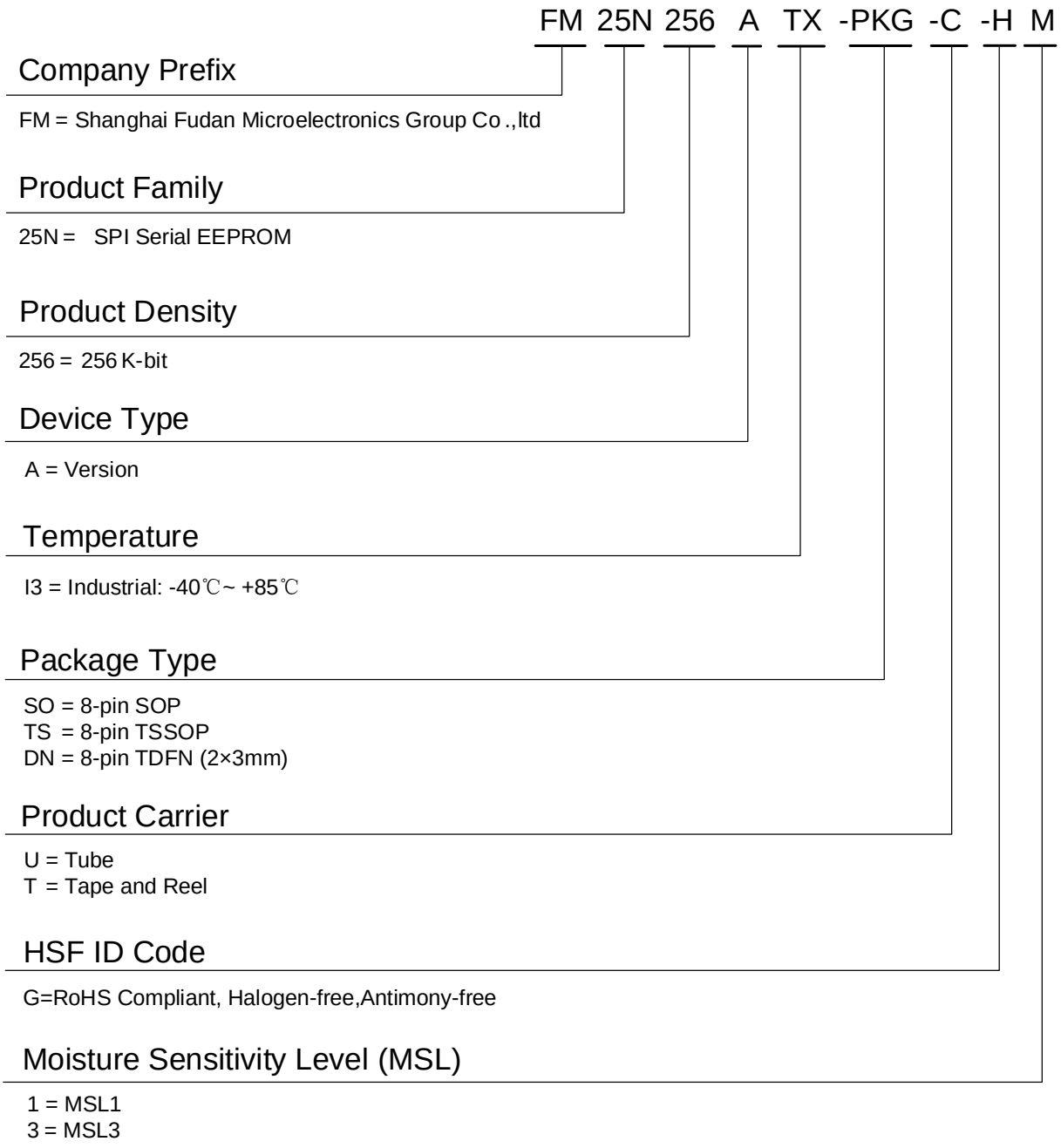
17.4. Cycling with Error Correction Code (ECC)

The FM25N256A offer an Error Correction Code (ECC) logic. The ECC is an internal logic function which is transparent for the 2-wire Serial communication protocol. The ECC logic is implemented on each group(1) of four EEPROM bytes. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved. Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group(1). As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in Section Cycling Performance By Groups Of Four Bytes on Page 20.

Note：

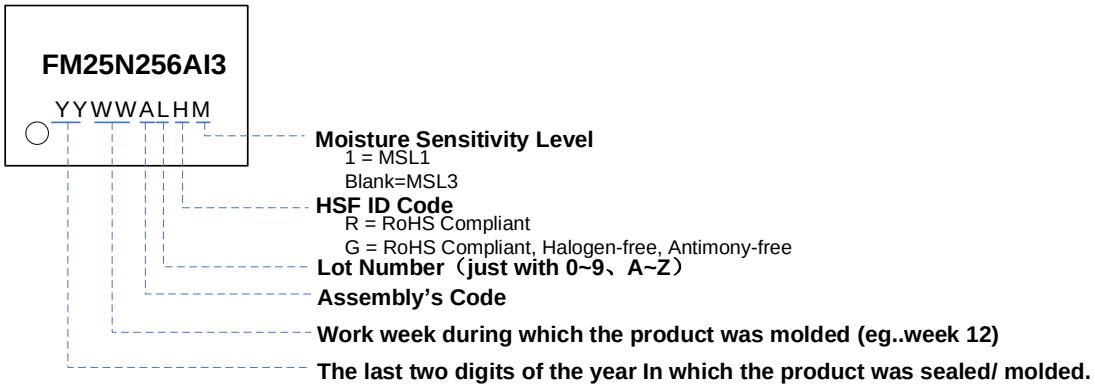
1. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.
2. For maximum endurance in applications that frequently rewrite data, it is recommended that users perform data write operations with groups of four data bytes as the smallest unit.

18. Ordering Information

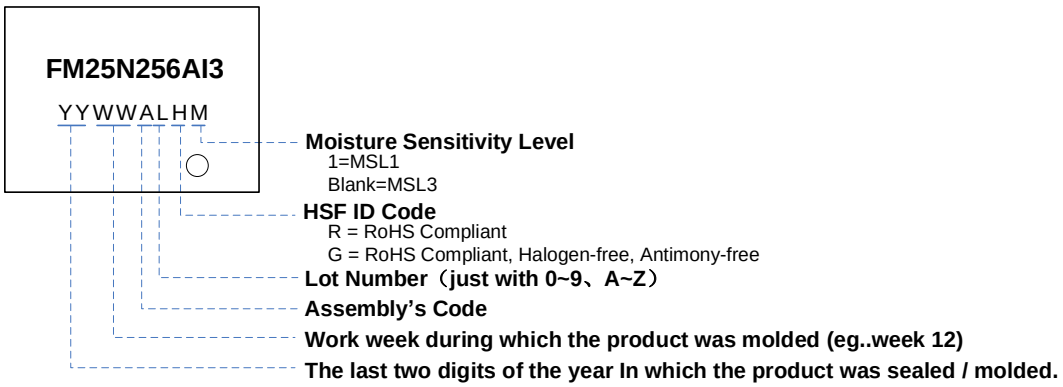


19. Part Marking Scheme

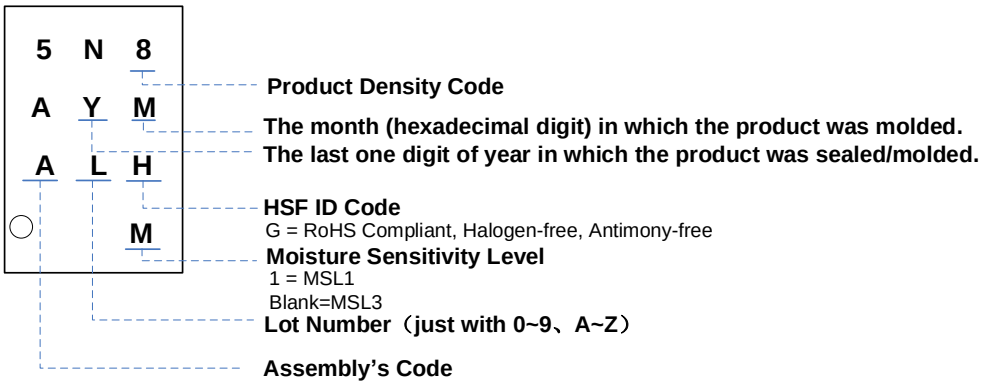
19.1. SOP8



19.2. TSSOP8

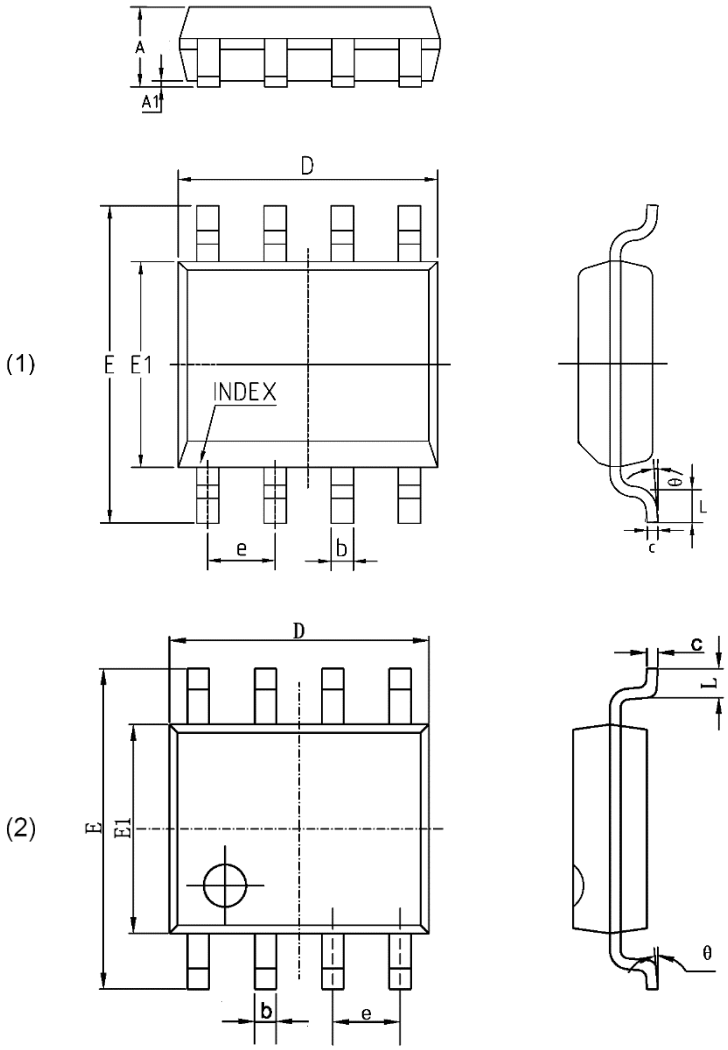


19.3. TDFN8



20. Packaging Information

SOP 8

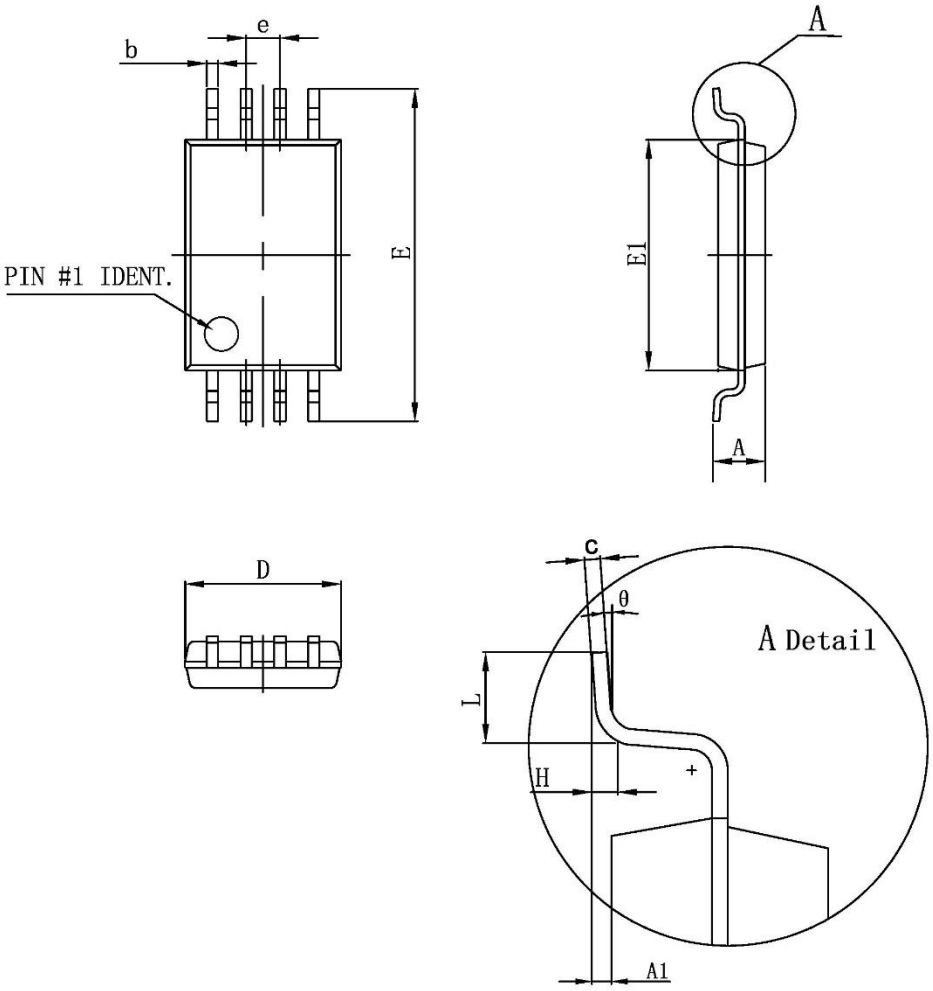


Symbol	MIN	MAX
A	1.350	1.750
A1	0.050	0.250
b	0.330	0.510
c	0.150	0.250
D	4.700	5.150
E1	3.700	4.100
E	5.800	6.200
e	1.270(BSC)	
L	0.400	0.900
θ	0°	8°

NOTE:

1. **Dimensions are in Millimeters.**

TSSOP8

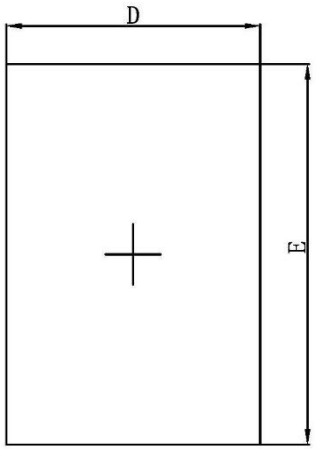


Symbol	MIN	MAX
D	2.900	3.100
E1	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E	6.200	6.600
A		1.200
A1	0.050	0.150
e	0.650 (BSC)	
L	0.450	0.750
θ	0°	8°

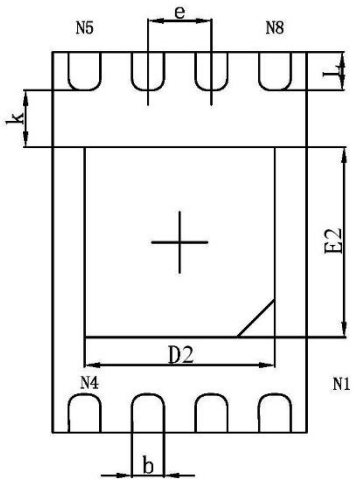
NOTE:

1. **Dimensions are in Millimeters.**

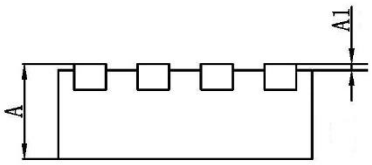
TDFN8(2x3mm)



Top View



Bottom View



Side View

Symbol	MIN	MAX
A	0.700	0.800
A1	0.000	0.050
D	1.900	2.100
E	2.900	3.100
D2	1.400	1.600
E2	1.400	1.700
k	0.150(MIN)	
b	0.180	0.300
e	0.500(TYP)	
L	0.200	0.500

NOTE:

1. **Dimensions are in Millimeters.**

21. Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Nov. 2023	29		Initial document Release.
1.1	Jan. 2024	29		1.Updated “5 Absolute Maximum Rating” 2.Updated “14.3 AC Characteristics” 3.Updated “Figure 19 Hold Timing” 4.Updated “15 Cycling Performance”

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